Dewar

Isolator & Bandpass Filter Module

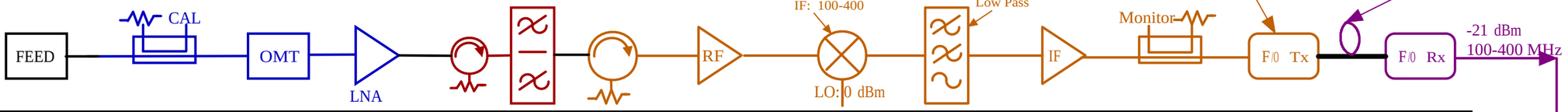
Downconverter

AC321-2.5
Noise floor:
-130 dBm /Hz

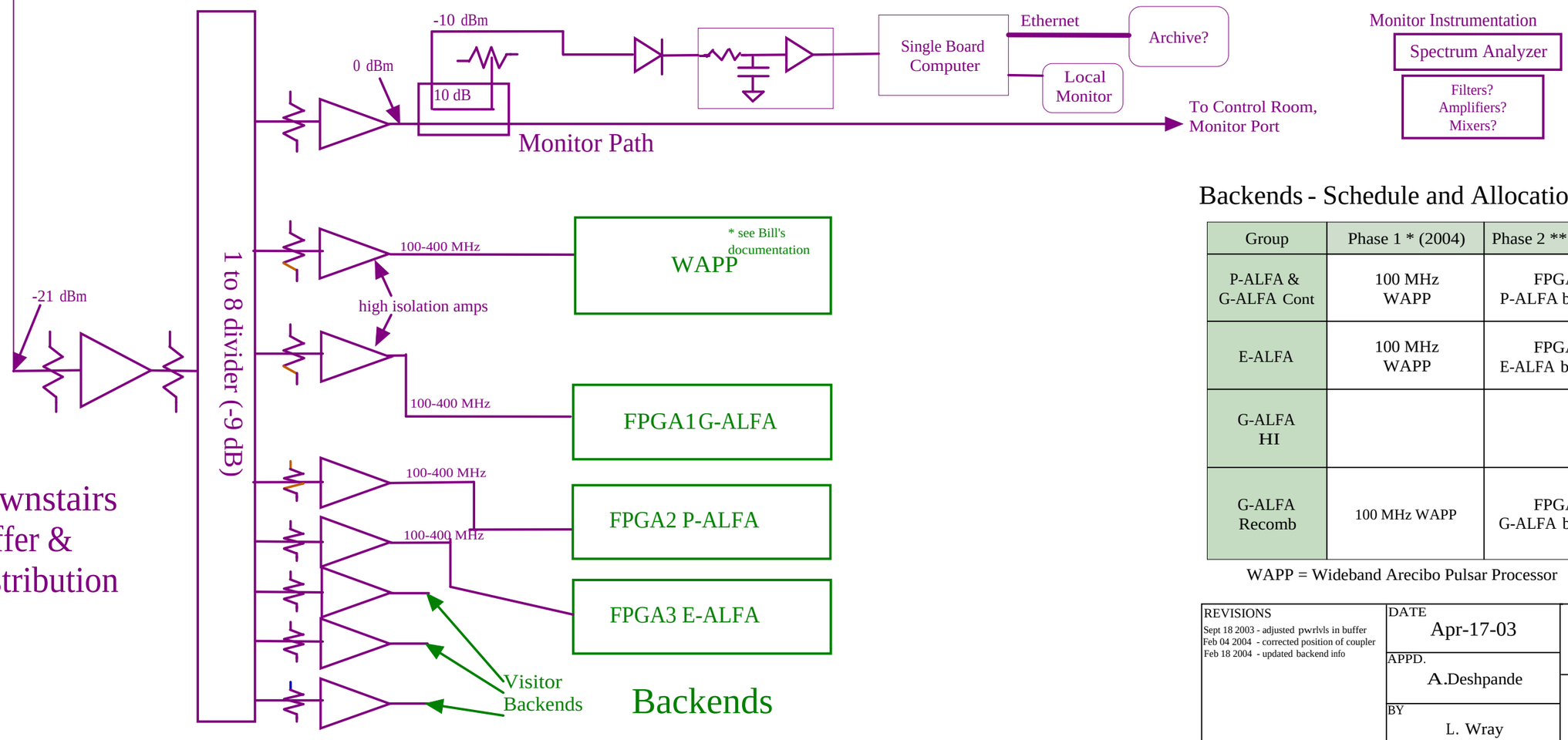
RF: 1225 - 1525
LO: 1625
IF: 100-400

700 MHz
Low Pass

0.4 dB/km x 1.2 km = 0.5 dB loss in fiber



1. Gain (-loss) (dB)		0	+40	-3 ?	-1	+23	+10	-1	+13	-1	-3 (tx and rx) + 0.5 (in fiber)
2. Cumulative noise power out in 300 MHz (dBm)			-59	-62	-63	-40	-30	-31	-18	-19	-21
3. Noise Figure (dB)	Spec: 6-8K at dewar flange, 3K for amp					+1.6	+15		+ 5		+25 dB
4. Teff	<------ 30K includes spillover and sky ------->				<---------- Downconverter stage measures 800K. Contributes < 1K to total Tsystem ---------->						
5. P1 (dBm)			+5			+6	+8		+13		+13
6. Headroom line 5 - line 2 (dB)			64			46	38		31		34



Backends - Schedule and Allocations

Group	Phase 1 * (2004)	Phase 2 ** (2005+)
P-ALFA & G-ALFA Cont	100 MHz WAPP	FPGA2 P-ALFA backend
E-ALFA	100 MHz WAPP	FPGA3 E-ALFA backend
G-ALFA HI		
G-ALFA Recomb	100 MHz WAPP	FPGA1 G-ALFA backend

WAPP = Wideband Arecibo Pulsar Processor

REVISIONS	DATE	ARECIBO OBSERVATORY CORNELL UNIVERSITY
Sept 18 2003 - adjusted pwrlvls in buffer Feb 04 2004 - corrected position of coupler Feb 18 2004 - updated backend info	Apr-17-03	
	APPD. A.Deshpande	ALFA RECEIVER and BACKEND SYSTEM BLOCK DIAGRAM One Channel of One Pixel
	BY L. Wray	