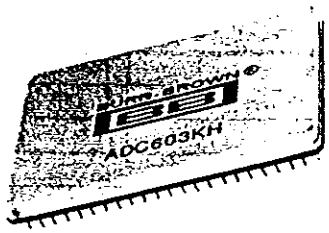
Appendix A:

MANUFACTURERS' DATA SHEETS

BURR-BROWN®



ADC603

12-Bit 10MHz Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- HIGH SPURIOUS-FREE DYNAMIC RANGE
- SAMPLE RATE: DC to 10MHz
- HIGH SIGNAL/NOISE RATIO: 68.2dB
- HIGH SINAD RATIO: 66dB
- LOW HARMONIC DISTORTION: –69.6dBc
- LOW INTERMOD. DISTORTION: –77.7dBc
- COMPLETE SUBSYSTEM: Contains Sample/Hold and Reference
- 46-PIN DIP PACKAGE
- 0°C TO +70°C AND –55°C TO +125°C

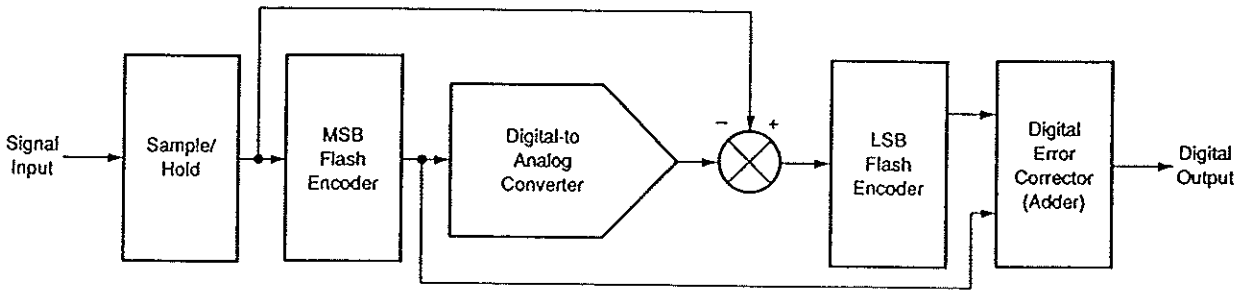
APPLICATIONS

- DIGITAL SIGNAL PROCESSING
- RADAR SIGNAL ANALYSIS
- TRANSIENT SIGNAL RECORDING
- FFT SPECTRUM ANALYSIS
- HIGH-SPEED DATA ACQUISITION
- IR IMAGING SYSTEMS
- DIGITAL RECEIVERS
- SIGINT, ECM, AND EW SYSTEMS
- DIGITAL OSCILLOSCOPES

DESCRIPTION

The ADC603 is an high performance analog-to-digital converter capable of digitizing signals at any rate from DC to 10 megasamples per second. Outstanding spurious-free dynamic range has been achieved by minimizing noise and distortion. Test summaries are furnished with each KH grade unit at no additional cost.

The ADC603 is a two-step subranging ADC subsystem containing an ADC, sample/hold amplifier, voltage reference, timing, and error-correction circuitry in a 46-pin hybrid DIP package. Logic is TTL. Two temperature ranges are available: 0°C to +70°C (JH, KH) and –55°C to +125°C (RH, SH).



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PDS-865C

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SPECIFICATIONS

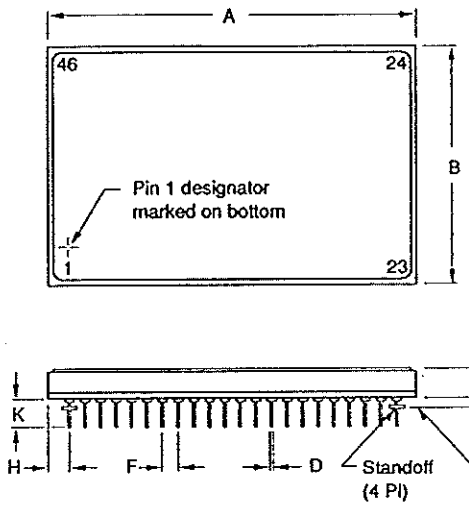
ELECTRICAL

T_C = +25°C, 10MHz sampling rate, R_S = 50Ω, $\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = −5.2V, and 15-minute warmup in convection environment, unless otherwise noted.

PARAMETER	CONDITIONS	ADC603JH			ADC603KH			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				12			12	Bits
INPUTS								
ANALOG								
Input Range	Full Scale	−1.25		+1.25	•		•	V
Input Impedance			1.5			•		MΩ
Input Capacitance			5			•		pF
DIGITAL								
Logic Family				TTL Compatible				
Convert Command	Start Conversion			Positive Edge				
Pulse Width	t = Conversion Period	10		t − 20	•		•	ns
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error	f = 200Hz		±0.2	1		±0.1	0.8	%FSR[1]
Input Offset	DC		±0.2	0.75		•	0.5	%FSR
Integral Linearity Error	f = 200Hz		0.75			0.5	1	LSB
Differential Linearity Error	f = 200Hz: 68.3% of all Codes		0.3			0.25	0.5	LSB
	99.7% of all Codes		0.4			0.3	0.65	LSB
	100% of all Codes		0.5	1		0.4	0.75	LSB
No Missing Codes			Guaranteed			Guaranteed		
Power Supply Rejection	$\Delta +V_{CC}$ = ±10%		±0.03			•	±0.07	%FSR/%
	$\Delta -V_{CC}$ = ±10%		±0.04			•	±0.07	%FSR/%
	$\Delta +V_{DD1}$ = ±10%		±0.004			•	±0.03	%FSR/%
	$\Delta -V_{DD2}$ = ±10%		±0.01			•	±0.03	%FSR/%
CONVERSION CHARACTERISTICS								
Sample Rate		DC		10M	DC		10M	Samples/s
Pipeline Delay	Logic Selectable		1, 2 or 3 Convert Command Periods					
DYNAMIC CHARACTERISTICS								
Differential Linearity Error	f = 4.9MHz: 68.3% of all Codes		0.3			•		LSB
	99.7% of all Codes		0.75			0.5		LSB
	100% of all Codes		1	1.25		0.6	0.9	LSB
Spurious Free Dynamic Range								
f = 5MHz (−0.5dB)	f_S = 9.99MHz		−72	−63		−74	−66	dB
Total Harmonic Distortion[2](THD)								
f = 5MHz (−0.5dB)	f_S = 9.99MHz		−68	−61		−69.6	−64	dBc[3]
f = 100kHz			−70	−65		−72.1	−68	dBc
Two-Tone Intermodulation Distortion[2,4]								
f = 2.2MHz (−6.5dB)	f_S = 8.006MHz		−75	−67		−77.7	−71	dBc
f = 2.5MHz (−6.5dB)								
Signal-to-Noise and Distortion (SINAD) Ratio								
f = 5MHz (−0.5dB)	f_S = 9.99MHz	60	65		62	66		dB
f = 100kHz (−0.5dB)		64	67		66	68.5		dB
Signal-to-Noise Ratio (SNR)								
f = 5MHz (−0.5dB)	f_S = 9.99MHz	63	67		66	68.2		dB
f = 100kHz (−0.5dB)		66	68		67	70.1		dB
Aperture Delay Time			−5			•	+9	ns
Aperture Jitter			9			•	20	ps rms
Analog Input Bandwidth (−3dB)								
Small Signal	−20dB Input		70		50	•		MHz
Full Power	0dB Input		40		30	•		MHz
Overload Recovery Time	2x Full-Scale Input		80			•	140	ns
OUTPUTS								
Logic Family				TTL Compatible				
Logic Coding	Logic Selectable		Two's Complement or Inverted Two's Complement					
Logic Levels	Logic LO, I_{OL} = −3.2mA	0	+0.3	+0.8	0	+0.3	+0.5	V
	Logic HI, I_{OH} = 160µA	+2.4	+3.5	+5	+2.4	+3.5	+5	V
EOC Delay Time	Data Out to DV	5	35		5	35		ns
Tri-State Enable/Disable Time	I_{OL} = −6.4mA, 50% In to 50% Out		37	100		37	100	ns
Data Valid Pulse Width		20	45	60	20	45	60	ns
POWER SUPPLY REQUIREMENTS								
Supply Voltages: $+V_{CC}$	Operating	+14.25	+15	+15.75	+14.25	+15	+15.75	V
$-V_{CC}$		−14.25	−15	−15.75	−14.25	−15	−15.75	V
$+V_{DD1}$		+4.75	+5	+5.25	+4.75	+5	+5.25	V
$-V_{DD2}$		−4.95	−5.2	−5.46	−4.95	−5.2	−5.46	V
Supply Currents: $+I_{CC}$	Operating		+60			+60	+80	mA
$-I_{CC}$			−60			−60	−80	mA
$+I_{DD1}$			+280			+280	+330	mA
$-I_{DD2}$			−565			−565	−630	mA
Power Consumption	Operating		6.1			6.1		W

MECHANICAL

H Package — Metal and Ceramic



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	2.370	2.420	60.20	61.47
B	1.560	1.610	39.62	40.89
C	.200	.260	5.08	6.60
D	.018 Dia BASIC		0.46 Dia BASIC	
F	.100 BASIC		2.54 BASIC	
H	0.75	.115	1.91	2.92
K	.150	.190	3.81	4.83
L	1.300 BASIC		33.02 BASIC	
M	—	10°	—	10°
N	.040	.060	1.02	1.52

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

PIN ASSIGNMENTS

1	Common (Case)	46	Common (Analog)
2	NC	45	Analog Signal In
3	$+V_{DD1}$ (+5V) Analog	44	$+V_{CC}$ (+15V) Analog
4	S/H Out	43	$-V_{CC}$ (–15V) Analog
5	A/D In	42	NC
6	$-V_{DD2}$ (–5.2V) Analog	41	NC
7	NC	40	NC
8	NC	39	DNC
9	Bit 1(MSB)	38	DNC
10	Bit 2	37	Gain Adjust
11	Bit 3	36	Offset Adjust
12	Bit 4	35	Common (Analog)
13	Bit 5	34	$+V_{CC}$ (+15V) Analog
14	Bit 6	33	$-V_{CC}$ (–15V) Analog
15	Bit 7	32	Common (Analog)
16	Bit 8	31	$-V_{DD2}$ (–5.2V) Digital
17	Bit 9	30	$+V_{DD1}$ (+5V) Analog
18	Bit 10	29	1 Pipeline Delay Select
19	Bit 11	28	0 Pipeline Delay Select
20	Bit 12 (LSB)	27	Output Logic Invert
21	$+V_{DD1}$ (+5V) Digital	26	Common (Digital)
22	Data Valid Output	25	Tri-State $\overline{\text{ENABLE}}$
23	Common (Digital)	24	Convert Command In

ORDERING INFORMATION

ADC603 ( ) H

Basic Model Number

Performance Grade Code
- J, K: 0°C to +70°C Case Temperature
- R, S: –55°C to +125°C Case Temperature

Package Code
- H: Metal and Ceramic

ABSOLUTE MAXIMUM RATINGS

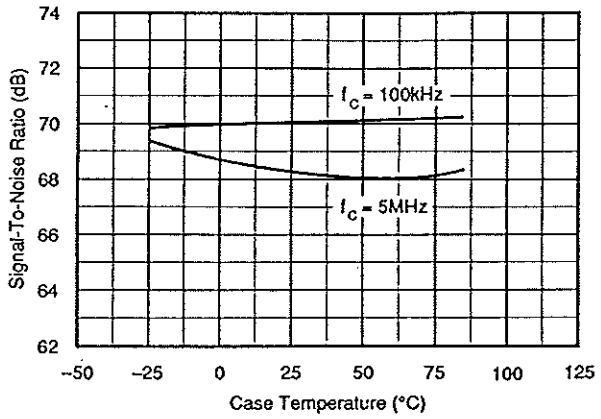
$\pm V_{CC}$	±16.5V
$+V_{DD1}$	+7V
$\pm V_{DD2}$	–7V
Analog Input	±5V
Logic Input	–0.5V to $+V_{DD1}$
Case Temperature	+125°C
Junction Temperature	+165°C
Storage Temperature	–65°C to +165°C

Stresses above these ratings may permanently damage the device.

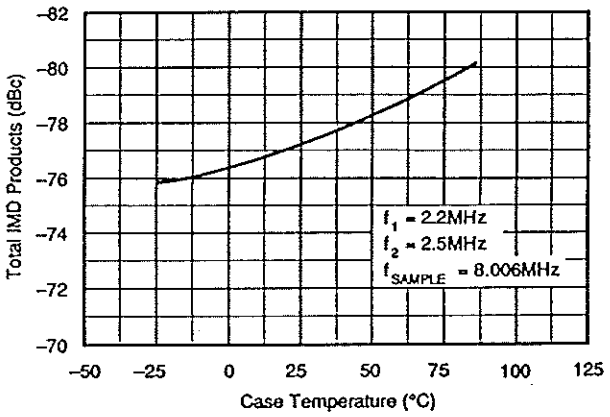
TYPICAL PERFORMANCE CURVES

$\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = −5.2V, R_S = 50Ω, 15-minute warmup, and T_C = +25°C, unless otherwise noted. All plots are 4096 point FFTs.

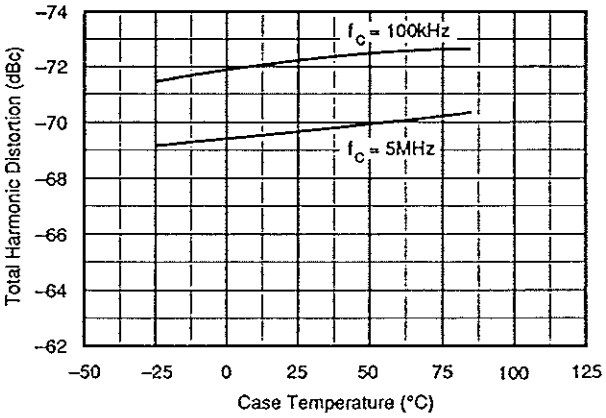
SIGNAL-TO-NOISE RATIO vs TEMPERATURE



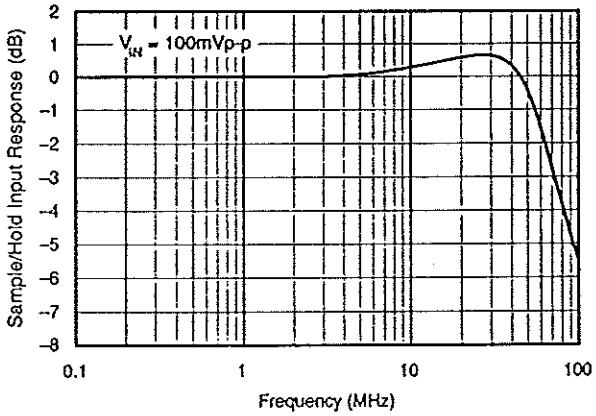
TWO-TONE IMD vs TEMPERATURE



TOTAL HARMONIC DISTORTION vs TEMPERATURE



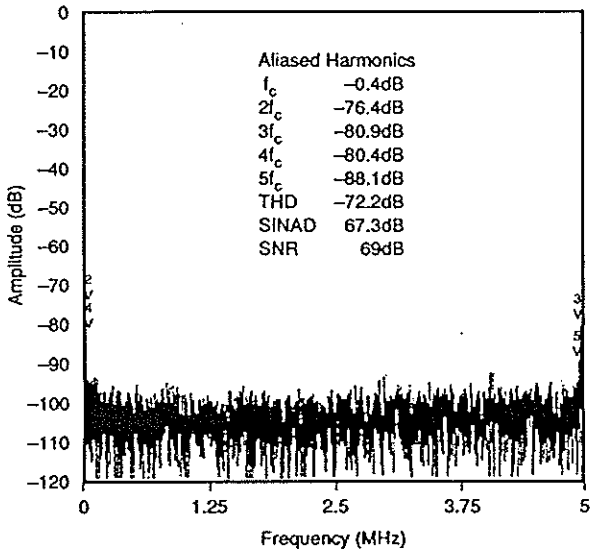
ANALOG INPUT BANDWIDTH



TYPICAL PERFORMANCE CURVES

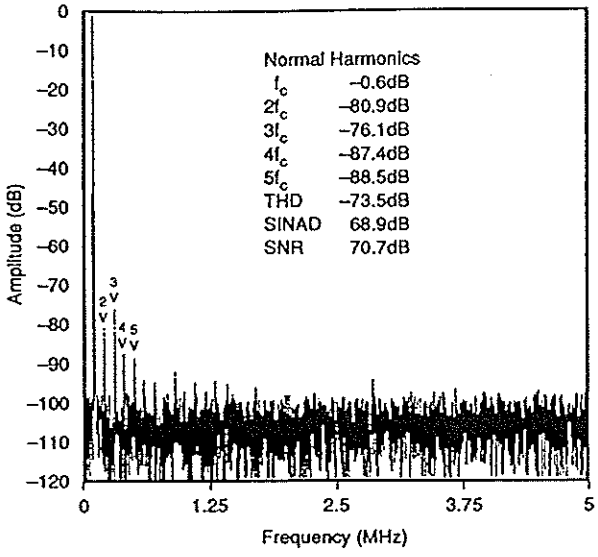
$\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = –5.2V, R_S = 50Ω, 10MHz sample rate, 15-minute warmup, and T_C = +25°C, unless otherwise noted. All plots are 4096-point FFTs.

5MHz HARMONIC DISTORTION



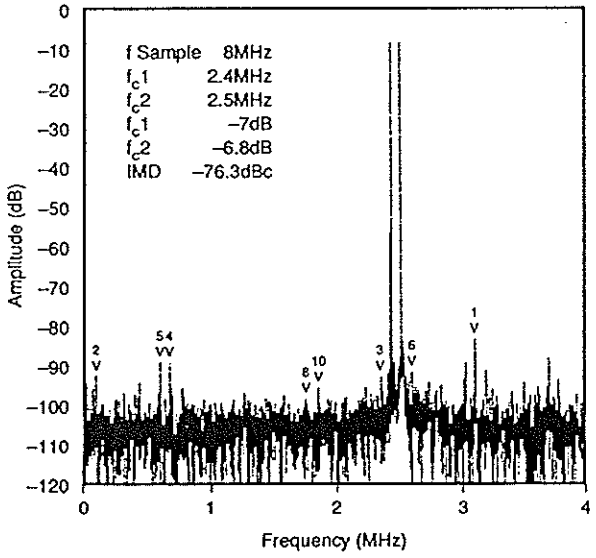
NOTE: Sample rate = 9.99 MHz; even harmonics folded to left edge and odd harmonics folded to right edge. Any non-harmonically related spurious products show clearly in the center.

100kHz HARMONIC DISTORTION



NOTE: Sample rate = 9.99 MHz; harmonics appear in normal order.

TWO-TONE INTERMODULATION DISTORTION



NOTE: Sample rate = 8MHz; highest IMD product is cursor number 1: f1 +f2. The second-order –76.3dBc product determines the wideband spurious-free dynamic range of this example. For RF applications third-order IMD products such as those at cursors 3 and 6 are the limiting spurs. Under these conditions spurious-free dynamic range is limited by 2f2+ f1 to 84.3dBc.

Sample rates of 10MHz show similar results.

TWO-TONE INTERMODULATION DISTORTION PRODUCTS

CURSOR	IMD	FREQUENCY	dB
1	2nd order : f1 + f2	3.086395621579MHz	–83.1
2	2nd order : f2 – f1	0.080140734949MHz	–91.4
3	3rd order : 2f1 – f2	2.339718530102MHz	–92.4
4	3rd order : 2f1 + f2	0.666536356529MHz	–88.4
5	3rd order : 2f2 – f1	0.586395621579MHz	–88.2
6	3rd order : 2f2 + f1	2.580140734949MHz	–91.1
7	4th order : 3f1 – f2	3.246677091478MHz	–109
8	4th order : 3f1 + f2	1.753322908522MHz	–100
9	4th order : 2f2 – 2f1	0.130281469898MHz	–114.8
10	4th order : 2f2 + 2f1	1.833463643471MHz	–95
11	4th order : 3f2 – f1	2.926114151681MHz	–115.4
12	4th order : 3f2 + f1	1.913604378421MHz	–98.2

NOTE: IMD products in this table are refered to full-scale (0dB). To refer IMD to carrier, subtract the larger of f_c1 or f_c2. In this example, IMD referred to carrier will be 6.8dB higher (worse) than the full-scale value shown.

THEORY OF OPERATION

The ADC603 is a two-step subranging analog-to-digital converter. This architecture is shown in Figure 1. The major system building blocks are: sample/hold amplifier, MSB flash encoder, DAC and error amplifier, LSB flash encoder, digital error corrector, and timing circuits. The ADC603 uses hybrid technology with laser-trimmed integrated circuits mounted in a multilayer ceramic package to integrate this complex circuit into a complete analog-to-digital converter subsystem with state-of-the-art performance.

Conceptually, the subranging technique is simple: sample and hold the input signal, convert to digital with a coarse ADC, convert back to analog with a coarse-resolution (but high-accuracy) DAC, subtract this voltage from the S/H output, amplify this "remainder," convert to digital with a second coarse ADC, and combine the digital output from the first ADC (MSB) with the digital output from the second ADC (LSB). In practice, however, achieving high conversion speed without sacrificing accuracy is a difficult task.

The analog input signal is sampled by a high-speed sample/hold amplifier with low distortion, fast acquisition time and very low aperture uncertainty (jitter). A diode bridge sampling switch is used to achieve an acceptable compromise between speed and accuracy. The diode bridge switching transients are buffered from the analog input by a high input impedance buffer amplifier. Since the hold capacitor does not appear in the feedback of the diode bridge output buffer, the capacitor can acquire the signal in 25ns. The low-bias-current output buffer is then required to settle to only the resolution (7 bits) of the first (MSB) flash encoder in 25ns, while an additional 60ns is allowed for settling to the resolution (12 bits) of the second (LSB) flash encoder. Sample/hold droop appears as only an offset error and does not effect linearity.

Both the MSB and the LSB flash encoder (ADC) function are performed by multiplexing one high-speed 7-bit resolution converter formed by parallel-connecting two 6-bit flash ADCs. The DAC voltage reference is also used to generate reference voltages for the MSB and LSB encoder to compensate drift errors. Buffering and scaling amplifiers are laser-trimmed to minimize voltage offset errors and optimize gain (input full-scale range) symmetry.

The subtraction DAC is an ECL 7-bit resolution monolithic DAC with 14-bit accuracy. Laser-trimmed thin-film nichrome resistors and high-speed bipolar circuitry allow the DAC output to settle to 14-bit accuracy in only 35ns.

A "remainder" or coarse conversion-error voltage is generated by resistively subtracting the DAC output from the output of the sample/hold amplifier. Before the second (LSB) conversion, the "remainder" is amplified by a wideband fast-settling two-input amplifier with a gain of 32V/V. To prevent overload on large amplitude transients, the active input is switched off to blank the amplifier input from the beginning of the S/H acquisition time to the end of the MSB encoder update time.

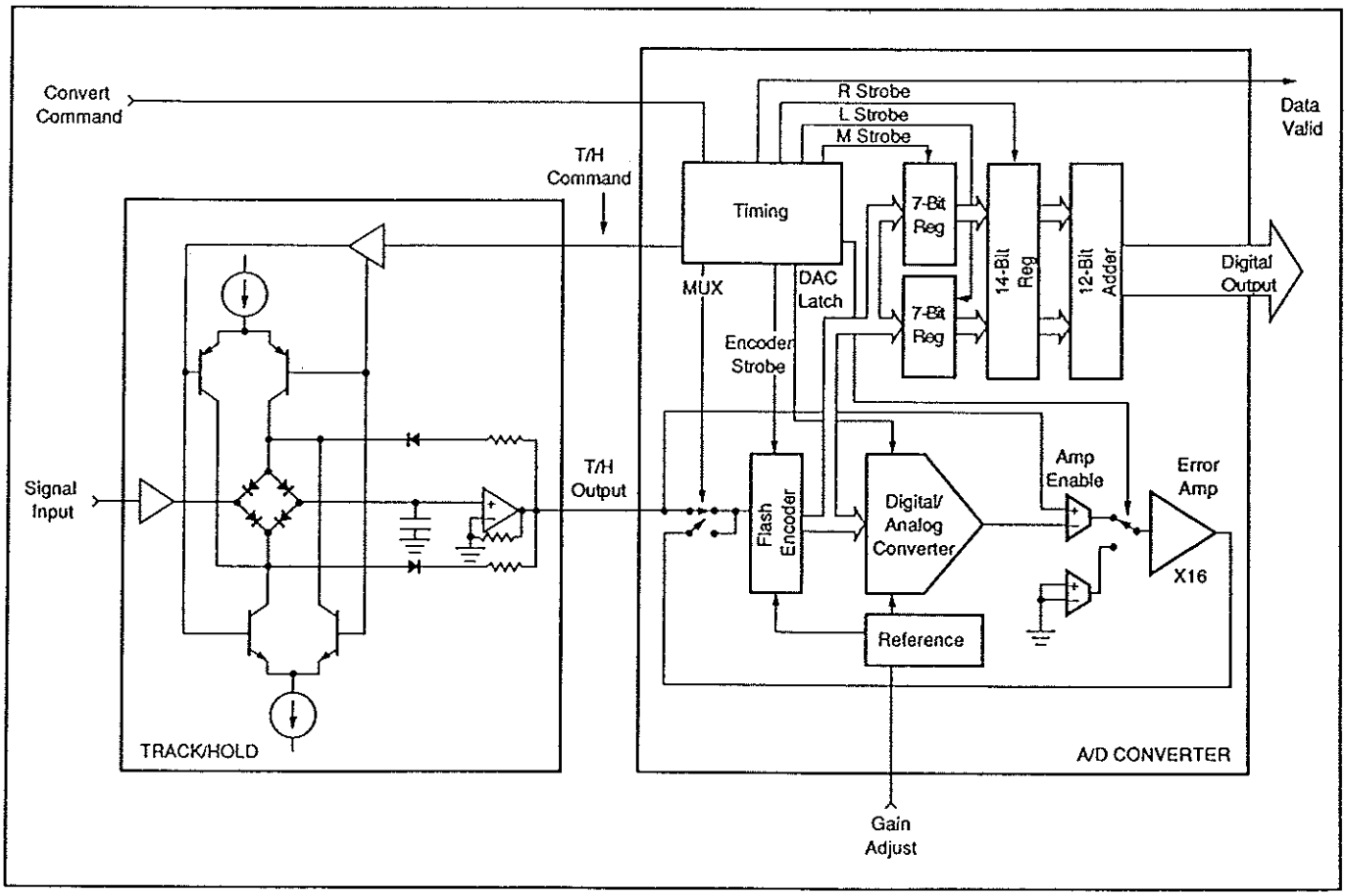


FIGURE 1. ADC603 Block Diagram—A Two-Step Subranging Architecture.

Internal timing circuits (ECL logic is used internally) supply all the critical timing signals necessary for proper operation of the ADC603. Some noncritical timing signals are also generated in the digital error correction circuitry. Timing signals are laser-trimmed for both pulse width and delay. ECL logic is used for its speed, low noise characteristics and timing delay stability over a wide range of temperatures and power supply voltages. Basic timing is derived from the output of a three-stage shift register driven by a synchronized 20MHz oscillator.

The convert command pulse is differentiated to allow triggering by pulses from as narrow as 10ns to as wide as 80% duty cycle.

The ADC603 timing technique generates a variable width S/H gate pulse which is determined by the conversion command pulse period minus a fixed 67ns ADC conversion time. ADC603 conversion rates are therefore possible somewhat above the 10MHz specification, but S/H acquisition time is sacrificed and accuracy is rapidly degraded. Converters with guaranteed operation at 10.24MHz sample rate are available on special order.

The output of the MSB and LSB encoders are read into separate 7-bit latches. The latched MSB data, along with the latched LSB data, is then read into a 14-bit latch after the leading edge of the LSB strobe and before being applied to the adder, where the actual error correction takes place. These latches eliminate any critical timing problems that could result when the converter is operated at the maximum conversion rate.

The function of the digital error correction circuitry is to assemble the 7-bit words from the two flash encoders into a 12-bit output word. A data valid (DV) pulse is also generated which is used to indicate when output data can be latched into an external register. This DV pulse is delayed 6ns after the output data has settled to allow sufficient set-up time for an external TTL data latch. A high-speed latch such as a 74F174 is recommended.

The 14-bit register output is then sent to a 12-bit adder where the final data output word is created. The MSB data forms the most significant seven bits of a 12-bit word, with the last five bits being assigned zeros. In a similar fashion, the LSB data from the least significant bits forms the other input to the adder, with the first five bits being assigned zeros. As two 12-bit words are being added, the output of the adder could exceed 12 bits in range; however, the final data output is only a 12-bit word, so a means of detecting an overrange is included to prevent reading erroneous data. The converter data output is forced to all ones for a full-scale input or overrange. The data output does not "roll-over" if the converter input exceeds its specified full-scale range of ±1.25V.

DISCUSSION OF PERFORMANCE

DYNAMIC PERFORMANCE TESTING

The ADC603 is a very high performance converter and careful attention to test techniques is necessary to achieve accurate results. Spectral analysis by application of a fast Fourier transform (FFT) to the ADC digital output will provide data on all important dynamic performance parameters: total harmonic distortion (THD), signal-to-noise ratio (SNR) or the more severe signal-to-noise-and-distortion ratio (SINAD), and intermodulation distortion (IMD).

A typical test setup for performing high-speed FFT testing of analog-to-digital converters is shown in Figure 2. Highly accurate phase-locked signal sources allow high resolution FFT measurements to be made without using window functions. By choosing appropriate signal frequencies and sample rates, an integral number of signal frequency periods can be sampled. As no spectral leakage results, a "rectangular" window (no window function) can be used. This was used to generate the typical FFT performance curves shown on page 5.

If generators cannot be phase-locked and set to extreme accuracy, a very low side-lobe window must be applied to the digital data before executing an FFT. A commonly used window such as the Hanning window is not appropriate for testing high performance converters; a minimum four-sample Blackman-Harris window is strongly recommended.[1] To

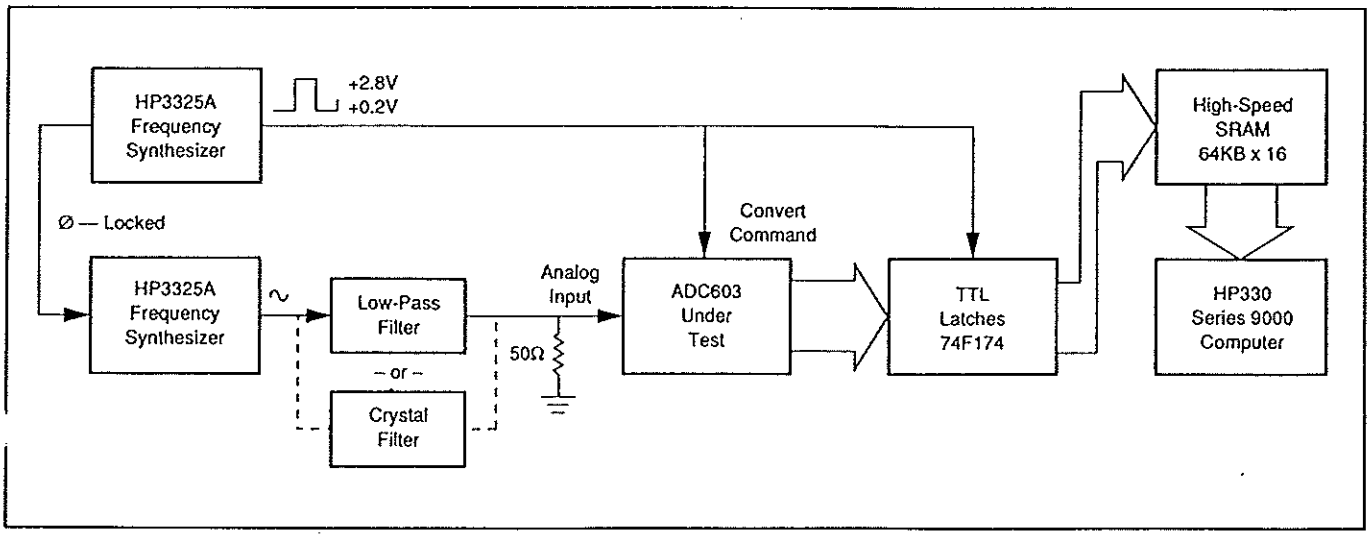
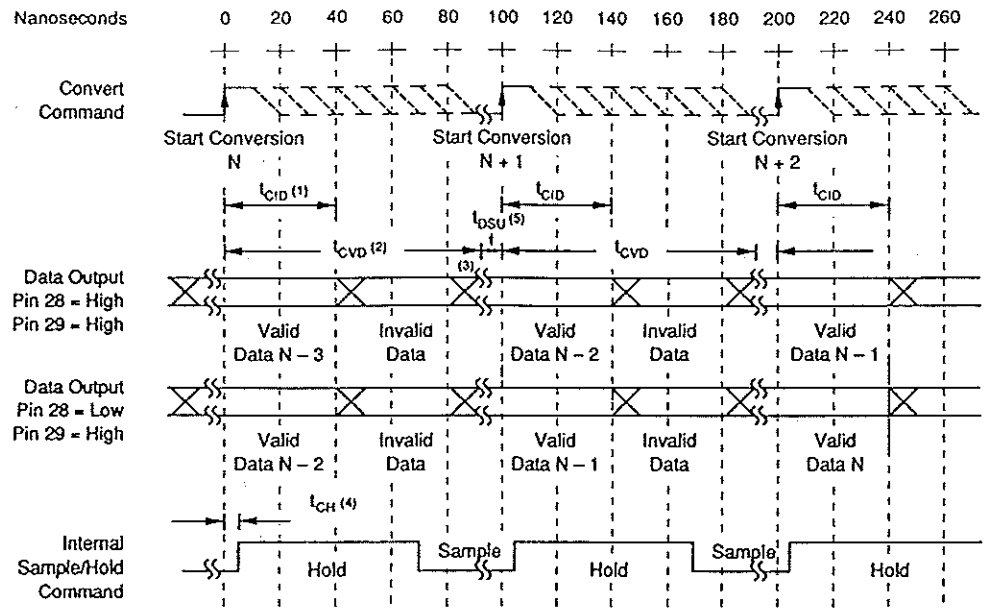


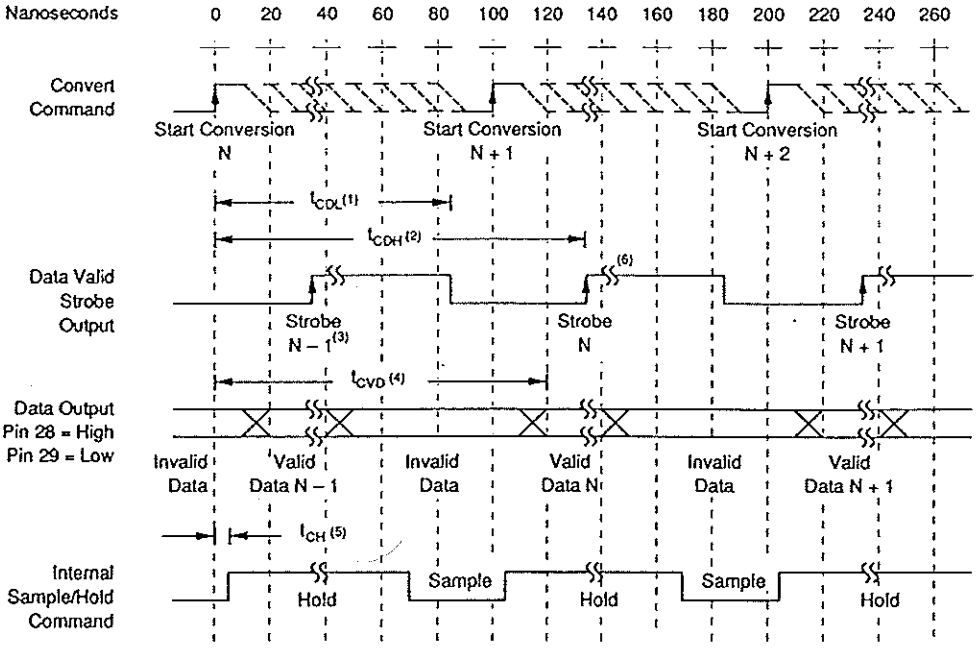
FIGURE 2. Block Diagram of FFT Test for THD, SNR, and SINAD.



NOTES: (1) t_{CID} = Delay time from Convert Command to Invalid Data. Typical value = 40ns. Independent of conversion rate. (2) t_{CVD} = Delay time from Convert Command to Valid Data. Typical value = 93ns. Independent of conversion rate. (3) The ⟆ symbol indicates the portion of the waveform that will "stretch out" at lower conversion rates. (4) t_{CH} = Delay time from Convert Command to the internal hold. Typical value = 6ns. Independent of conversion rate. (5) t_{DSU} = data set-up time. This depends on conversion rate and may be calculated by:

$$t_{DSU} = \frac{1}{f_{SAMPLE}} - t_{CVD}$$

FIGURE 13. Convert Command Strobe Timing.



NOTES: (1) t_{CDL} = Delay time from Convert Command to the falling edge of Data Valid Strobe. Typical value = 85ns. Independent of conversion rate. (2) t_{CDH} = Delay time from Convert Command to the rising edge of Data Valid Strobe. Typical value = 135ns. Independent of conversion rate. (3) If Conversion "N" is the first conversion, then there is no Strobe N-1, and the Data Valid Strobe Signal will simply be high until t_{CDL} after the first Convert Command. (4) t_{CVD} = delay time from Convert Command to Valid Data. Typical value = 120ns. Independent of conversion rate. (5) t_{CH} = Delay time from Convert Command to Internal Hold Command. Typical value = 6ns. Independent of conversion rate. (6) The ⟆ symbol indicates the portion of the waveform that will "stretch out" at lower conversion rates.

FIGURE 14. Data Valid Strobe Timing.

Pin 28 is used to control the amount of pipeline delay. If pin 28 is held LO, then output data "N – 2" will be valid on the rising edge of Convert Command "N." If pin 28 is held HI, then output data "N – 3" will be valid on the rising edge of Convert Command "N." These timing relationships are valid at any conversion rate up to 10MHz. At rates approaching 10MHz, however, the data setup time before the rising Convert Command edge may become as short as 6ns. Therefore, the use of high-speed TTL latches such as the 74F174 hex flip-flop is recommended to capture the data. If slower latches must be used, then the setup time can effectively be improved by adding several nanoseconds of delay between the Convert Command and the latch clock signal.

Data Valid Timing Option (pin 29 = LO)

With this option, data from conversion "N" becomes valid after a fixed delay from the rising edge of Convert Command "N." The delay is approximately 135ns, at which time the Data Valid strobe signal will rise. This signal may be connected directly to the clock input of the user's data latch.

See Figure 18 for timing relationships. Pin 28 must be left HI at all times when using the Data Valid timing option.

The advantages of this method are that no subsequent conversions are required in order to read the data, and the data is available as soon as possible after the start of conversion. Therefore, the Data Valid option is most useful in systems where the ADC may be operated asynchronously, or where the very first data latch output after power-up must represent a valid conversion. Note that because the delay is fixed at approximately 135ns independent of conversion rate, the Data Valid pulse will overlap into the next conversion at rates above 7.4MHz. This does not preclude proper operation at any rate up to 10MHz.

DATA OUTPUT

Output logic inversion can be accomplished by programming pin 27. Binary Two's Complement or Inverted Binary Two's Complement output data formats are available (Table II).

The ADC603 output logic is TTL compatible. The tri-state output is controlled by $\overline{\text{ENABLE}}$ pin 25. For normal operation, pin 25 will be tied LO. A logic HI on pin 25 will switch the ouput data register to a high-impedance state (Figure 20). Output OFF leakage current I_{OZL} and I_{OZH} will be less than 50µA over the converter's specified operating temperature range. Tri-state output should be isolated from noisy digital bus lines, since the noise can couple back through the OFF data register and create noise in the ADC.

DIGITAL INPUTS

Logic inputs are TTL compatible. Open inputs will assume a HI logic state; unused inputs may be allowed to float or they may be tied to an appropriate TTL logic level.

PIN NUMBER	DATA LATCHED BY CONVERT COMMAND		DATA LATCHED BY DATA VALID STROBE
	N–3	N–2	N–1
28	HI	LO	HI
29	HI	HI	LO

TABLE I. Pipeline Delay Selection Logic.

NOTES:

1. *FAST™ Applications Handbook*, 1987. Fairchild Semiconductor Corp.
2. *Fairchild Advanced CMOS Technology*, Technology Seminar Notes, 1985.
3. "Impedance Matching Tweaks Advance CMOS IC Testing", Gerald C. Cox, *Electronic Design*, April, 1987.
4. "Grounding for Electromagnetic Compatibility", Jerry H. Boogar, *Design News*, 23 February, 1987.

OFFSET AND GAIN ADJUSTMENT

The ADC603 is carefully laser-trimmed to achieve its rated accuracy without external adjustments. If desired, both gain error and input offset voltage error may be trimmed to zero with external potentiometers (Figure 23). Trim range is typically 2%; large offsets and gain changes should be made elsewhere in the system. Using an input buffer amplifier allows a convenient point for injecting large offset voltages and making wide gain adjustments.

If offset and gain trim is not used, pins 36 and 37 should be left unconnected.

THERMAL REQUIREMENTS

The ADC603 is tested and specified over a temperature range of 0°C to +70°C (J, K grade) and –55°C to +125°C (R, S grade). The converters are tested in a forced-air environment with a 10 SCFM air flow. With a small heat sink (Figure 24) the ADC603 can be operated in a normal convection ambient-air environment if submodule case temperature does not exceed the upper limit of its specification.[1]

High junction temperature can be avoided by using forced-air cooling, but it is not required at moderate ambient

INPUT VOLTAGE (Exact Center of Code)	DIGITAL DATA OUTPUT LOGIC CODING	
	Binary Two's Complement (BTC) Pin 27 = LO	Inverted Binary Two's Complement (BTC) Pin 27 = HI
	MSB LSB	MSB LSB
+FS (+1.25V)	011111111111*	100000000000*
+FS – 1LSB (+1.2494V)	011111111111	100000000000
+FS – 2LSB (+1.2488V)	011111111110	100000000001
+3/4FS (+0.9375V)	011000000000	100111111111
+1/2FS (+0.625V)	010000000000	101111111111
+1/4FS (+0.3125V)	001000000000	110111111111
+1LSB (+610µV)	000000000001	111111111110
Bipolar Zero (0V)	000000000000	111111111111
–1LSB (–610µV)	111111111111	000000000000
–1/4FS (–0.3125V)	111000000000	000111111111
–1/2FS (+0.625V)	110000000000	001111111111
–3/4FS (–0.9375V)	101000000000	010111111111
–(FS – 1LSB) (–1.2494V)	100000000001	011111111110
–FS (–1.25V)	100000000000	011111111111

* Indicates overrange condition.

TABLE II. Digital Data Output Logic Coding.

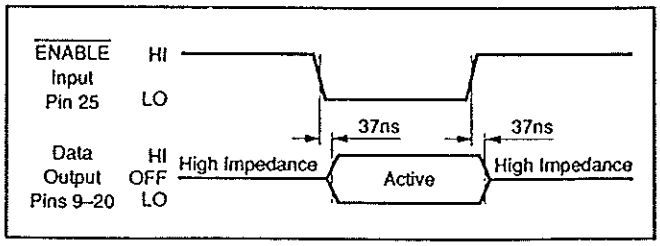


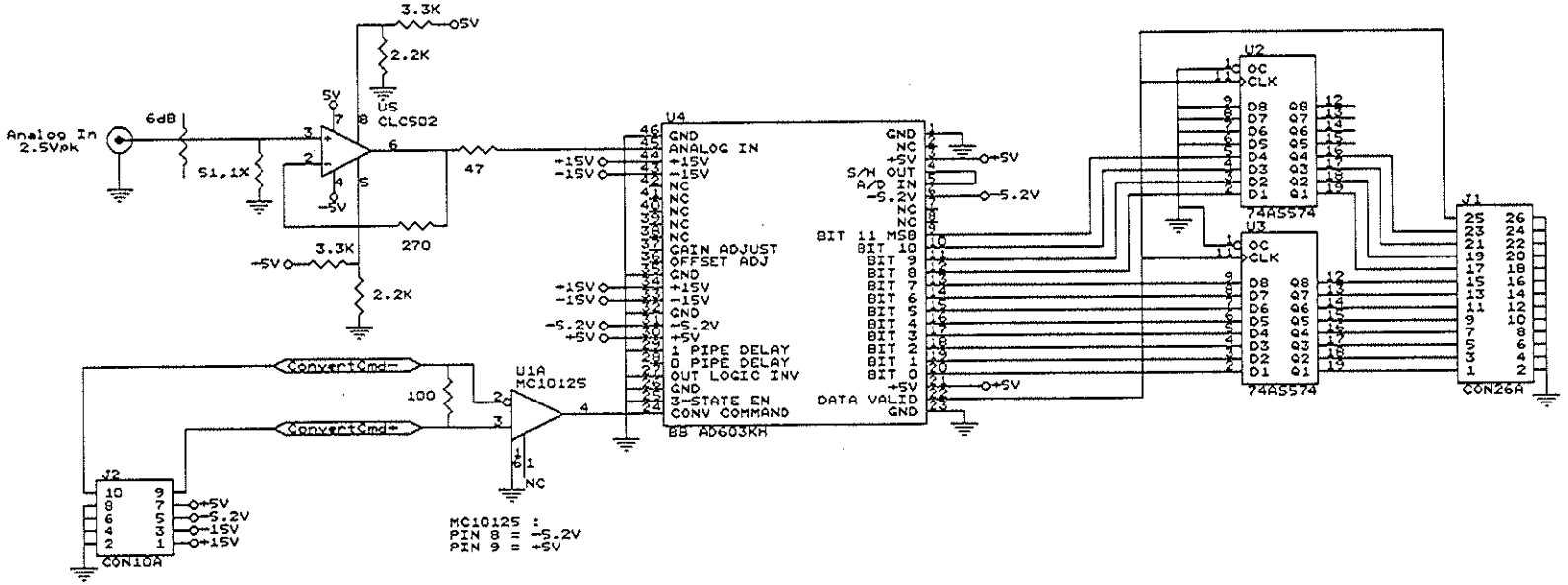
FIGURE 22. Digital Data Tri-State Output.

Appendix B:

Schematics

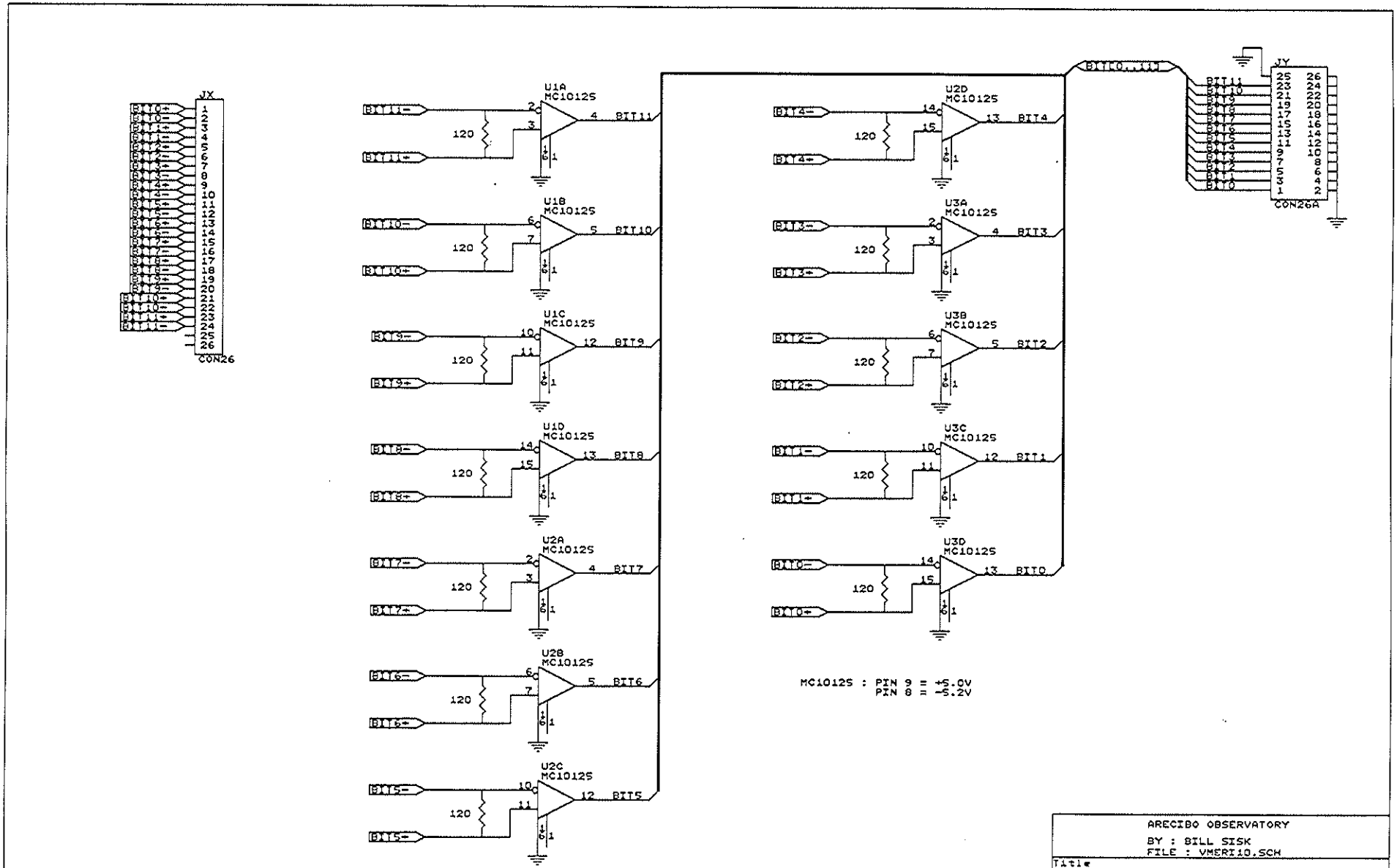
```
!LINK
!VMERI1.SCH          Block Diagram
!VMERI2.SCH            "
!VMERI3.SCH          Interconnections Block Diagram
!VMERI4.SCH          Flow Chart for Data Transfer

!VMERI9.SCH          RI1: AD CONVERTER
!VMERI10.SCH         RI1: DIGITAL INPUT TEST BOARD
!VMERI11.SCH         RI2: I1 Packer
!VMERI12.SCH              Q1 PACKER
!VMERI13.SCH              I2 PACKER
!VMERI14.SCH              Q2 PACKER
!VMERI15.SCH         RI3: INPUT PULSE GENERATOR
!VMERI16.SCH         RI4: SAMPLE PULSE GENERATOR
!VMERI17.SCH              "
!VMERI18.SCH              "

                     RI5: CONTROLLER
!VMERI20.SCH              SERIAL RECEIVER
!VMERI21.SCH              COMMAND BITS DECODER
!VMERI22.SCH              SAMPLER CONFIGURATION WORD
!VMERI23.SCH              MEMORY WRITE, SEQUENCE LENGTH, GW LENGTH
!VMERI24.SCH              AUXILIARY STATUS WORD / LOOPBACK
!VMERI25.SCH              SERIAL TRANSMITTER
!VMERI26.SCH              POWER SUPPLY MONITOR
!VMERI27.SCH              RECEIVER NETWORK
!VMERI28.SCH              UNUSED GATES

!VMERI30.SCH         RI6: POWER SUPPLIES
!VMERI31.SCH         RI7: CONNECTOR DIAGRAM
!VMERI32.SCH              "
!VMERI33.SCH              "

!VMERI35.SCH         RI8: FIFO BOARD
!VMERI36.SCH              "
!VMERI37.SCH              "
!VMERI38.SCH              "
!VMERI39.SCH              "
!VMERI40.SCH              "
!VMERI41.SCH              "
```

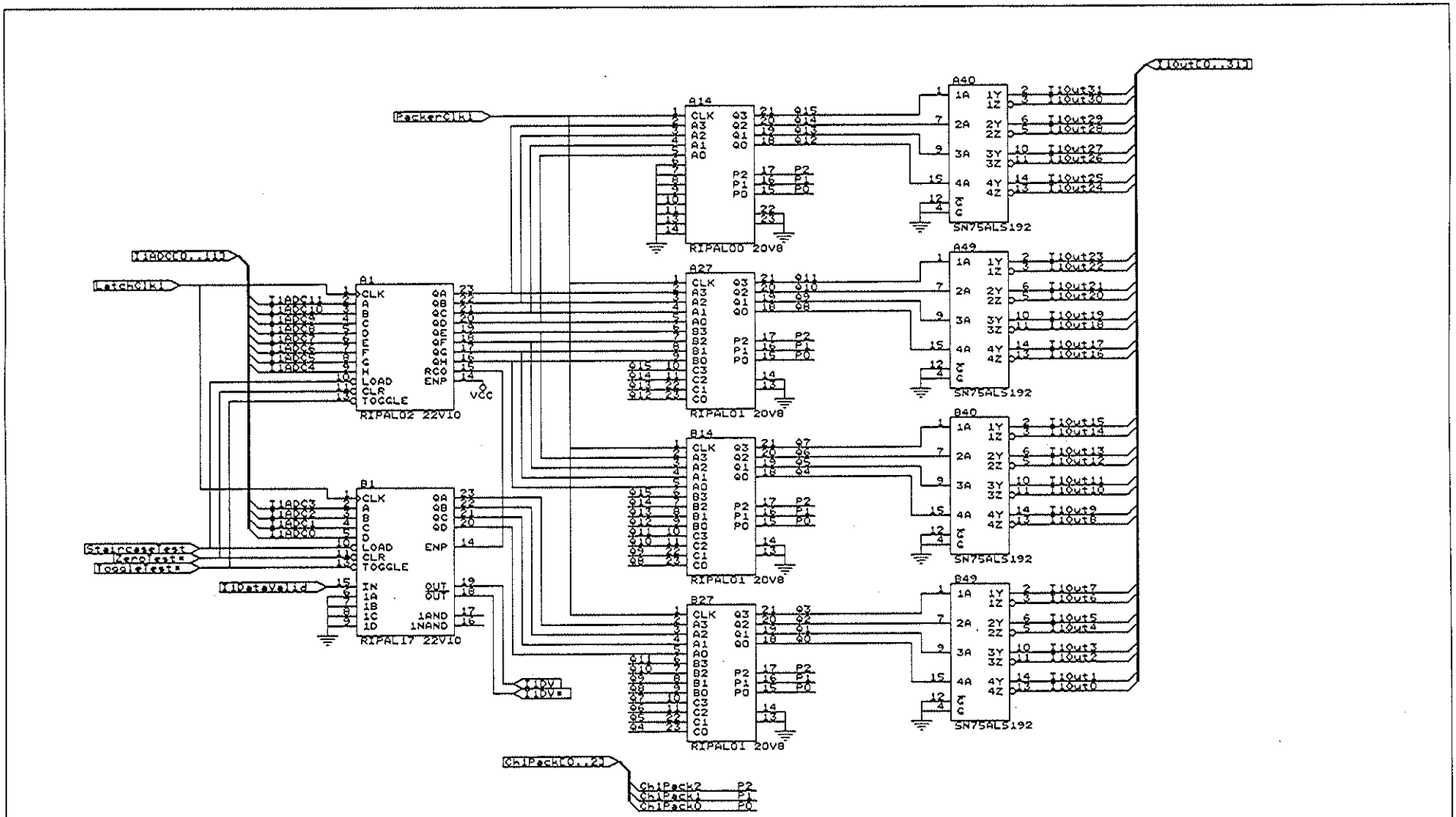
	ARECIBO OBSERVATORY
	BY : BILL SISK
Title	VME BASED RADAR INTERFACE
Size: B	Document Number:	REV: 0
Date: January 17, 1994	Sheet of



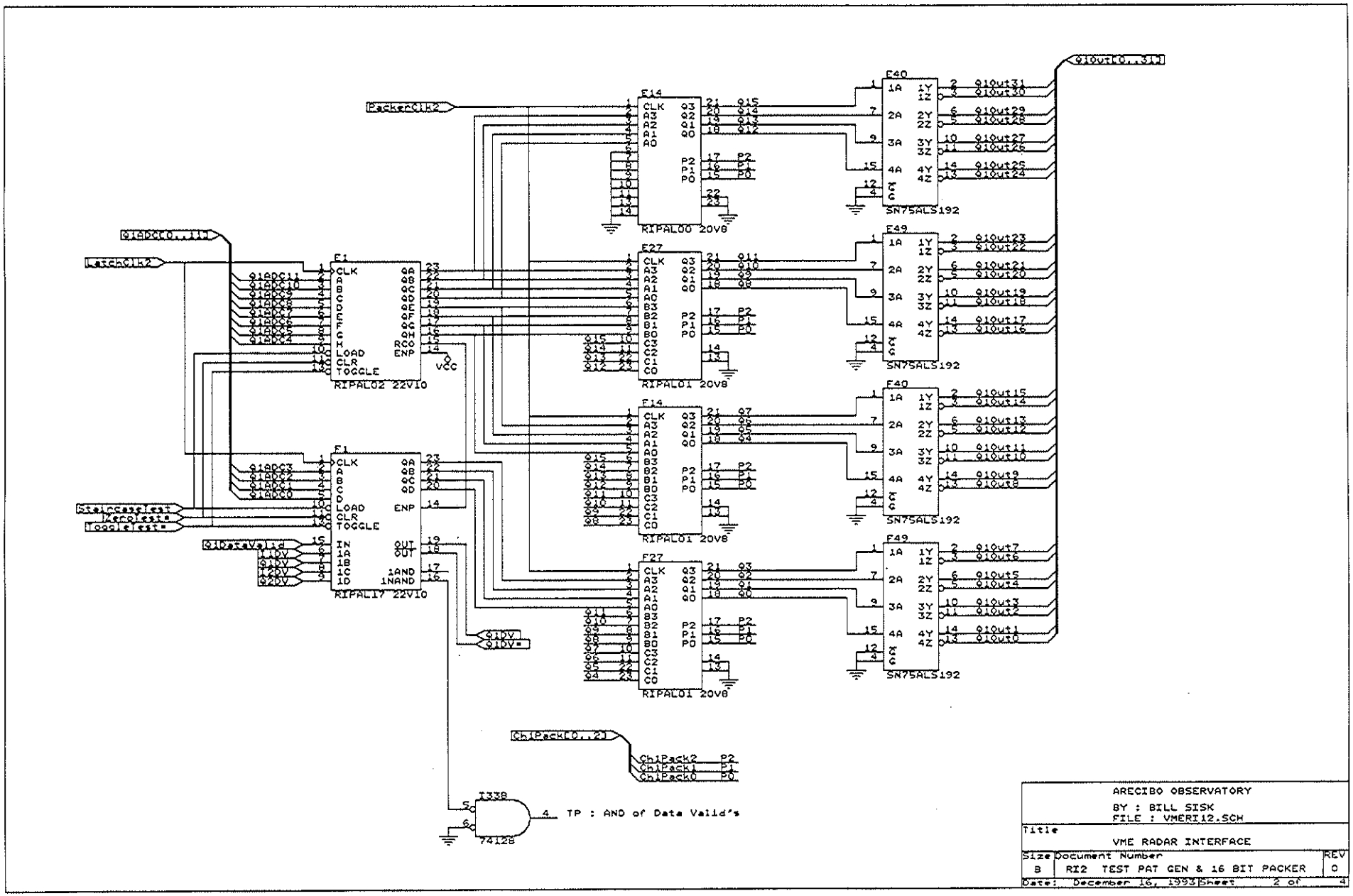
2.2uF & .01uF capacitors on all power pins.

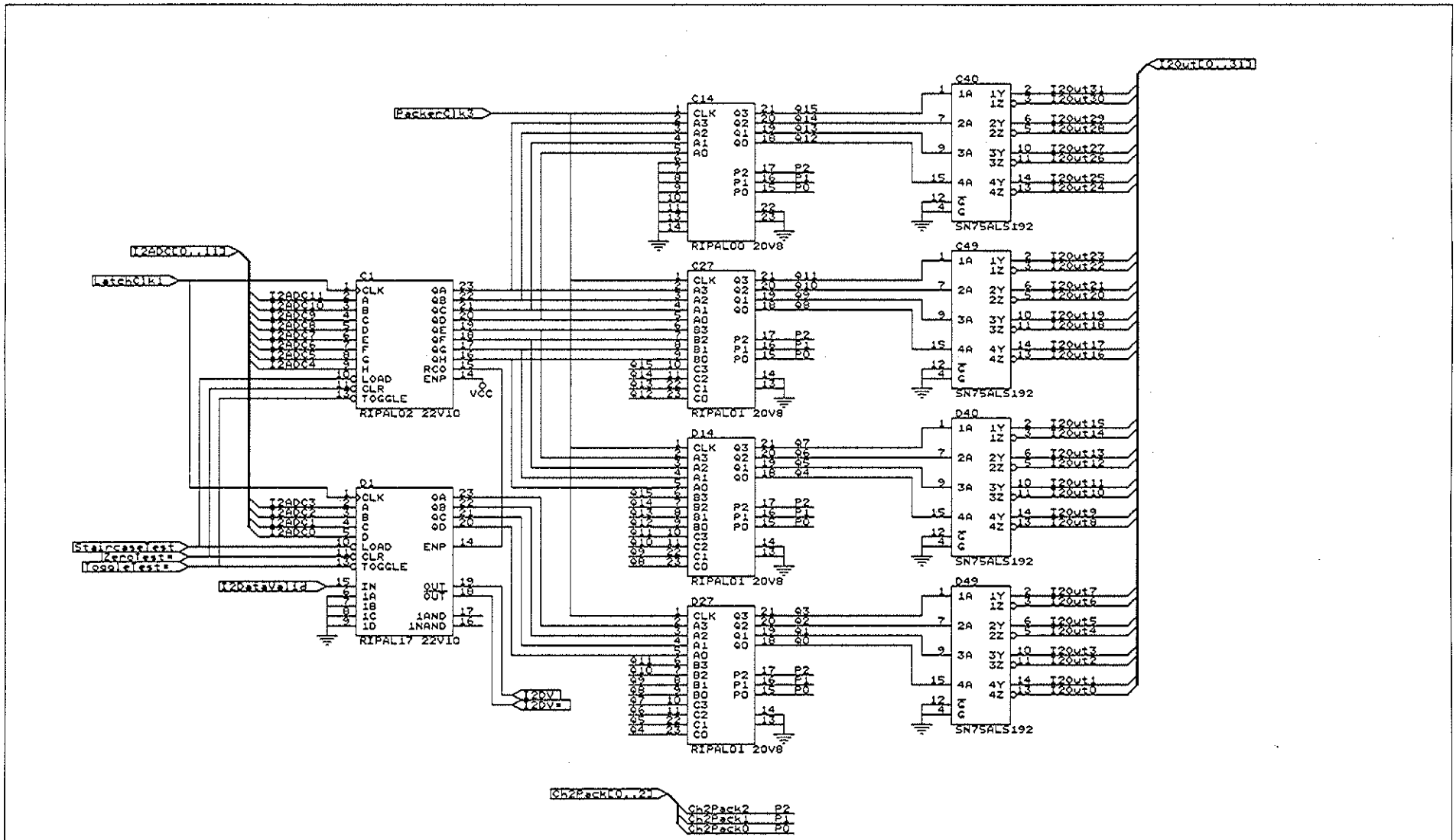
ARECIBO OBSERVATORY		
BY : BILL SISK		
FILE : VMERI9.SCH		
Title: VME RADAR INTERFACE		
Size: B	Document Number: RI1 A-TO-D CONVERTER	REV
Date: December 16, 1993	Sheet 1 of 2	


JX
CON26
U1A MC10125
U1B MC10125
U1C MC10125
U1D MC10125
U2A MC10125
U2B MC10125
U2C MC10125
U2D MC10125
U3A MC10125
U3B MC10125
U3C MC10125
U3D MC10125
120
BIT11+
BIT11-
BIT10+
BIT10-
BIT9+
BIT9-
BIT8+
BIT8-
BIT7+
BIT7-
BIT6+
BIT6-
BIT5+
BIT5-
BIT4+
BIT4-
BIT3+
BIT3-
BIT2+
BIT2-
BIT1+
BIT1-
BIT0+
BIT0-
BIT0..11
JY
CON26A
MC10125 : PIN 9 = +5.0V
PIN 8 = -5.2V
ARECIBO OBSERVATORY
BY : BILL SISK
FILE : VMERI10.SCH
Title
VME RADAR INTERFACE
Size B
Document Number
RI1 DIGITAL INPUT TEST BOARD
REV 0
Date: December 17, 1993
Sheet 2 of 2



ARECIBO OBSERVATORY		
BY : BILL SISK		
FILE : VMERI11.SCH		
Title: VME RADAR INTERFACE		
Size: B	Document Number: RI2 TEST PAT GEN & 16 BIT PACKER	REV: 0
Date: December 16, 1993	Sheet 1 of 4	


PackerClk2
Q10DC[0..11]
LatchClk2
F1
RIPAL02 22V10
F14
RIPAL00 20V8
F27
RIPAL01 20V8
F40
SN75ALS192
F49
SN75ALS192
Q10out[0..31]
Q10DataValid
RIPAL17 22V10
Q10V
Q10V=
ChiPack[0..2]
ChiPack2
ChiPack1
ChiPack0
I338
74128
TP : AND of Data Valid's
ARECIBO OBSERVATORY
BY : BILL SISK
FILE : VMERI12.SCH
Title
VME RADAR INTERFACE
Size B
Document Number RI2 TEST PAT GEN & 16 BIT PACKER
REV 0
Date: December 16, 1993 Sheet 2 of 4



	ARECIBO OBSERVATORY
	BY : BILL SISK
	FILE : VMERI13.SCH
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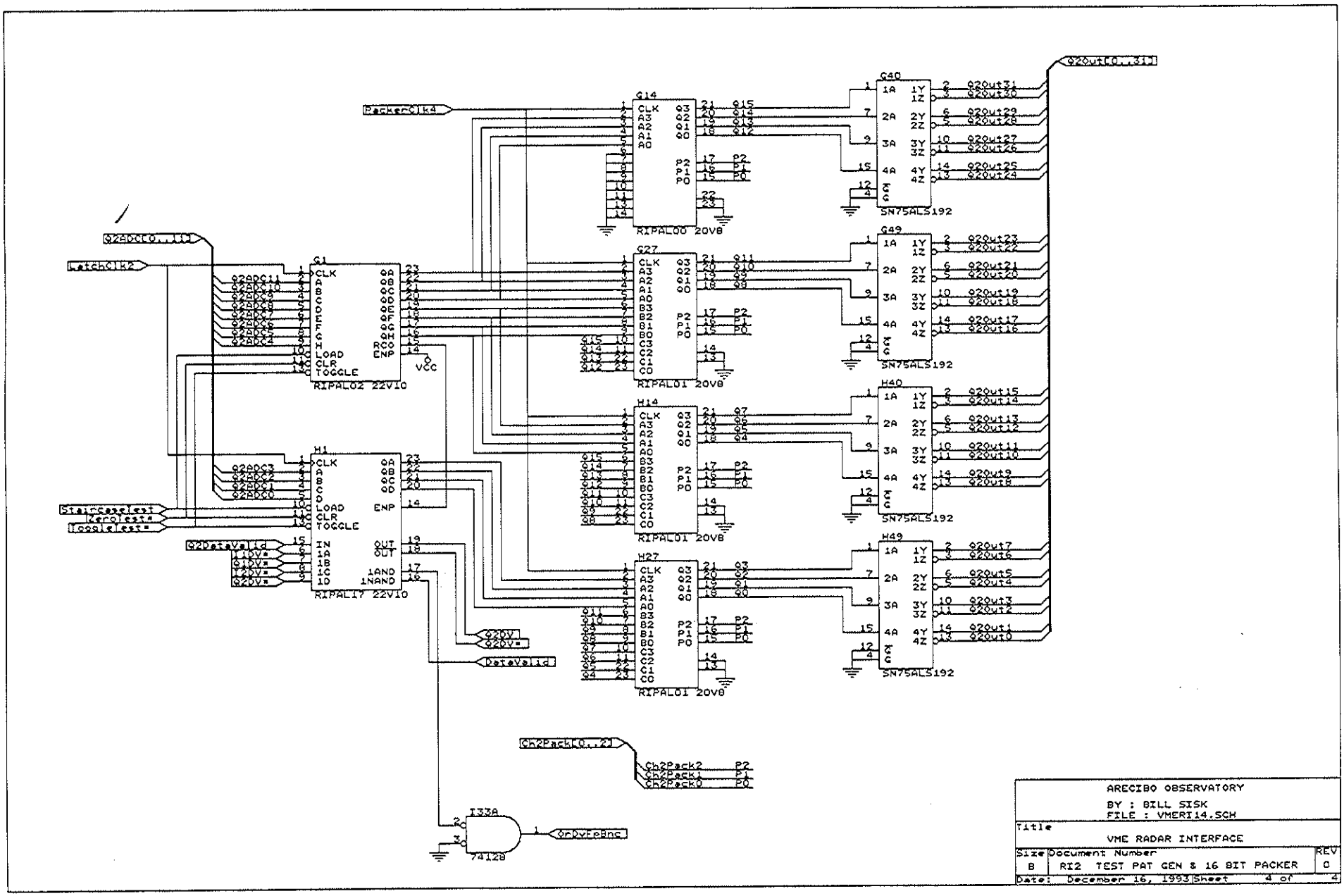
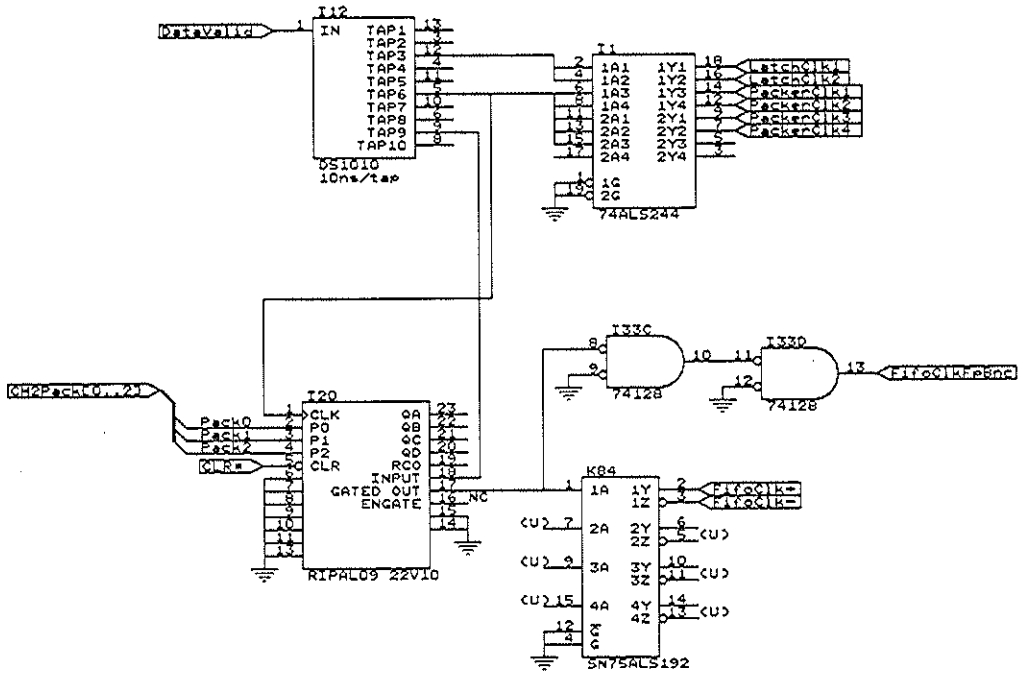
Size: B	Document Number: RI2 TEST PAT GEN & 16 BIT PACKER — REV: 0
Date: December 16, 1993	Sheet 3 of 4


PackerClk4
G14
RIPAL00 20V8
G40
SN75ALS192
G920ut[0..31]
G920DC[0..11]
LatchClk2
G1
RIPAL02 22V10
VCC
G27
RIPAL01 20V8
G49
SN75ALS192
H40
H14
RIPAL01 20V8
SN75ALS192
H1
RIPAL17 22V10
StairCaseTest
ZeroTest*
ToggleTest*
G20DataValid
G20V
G20V*
DataValid
H27
RIPAL01 20V8
H49
SN75ALS192
Ch2Pack[0..2]
I33A
74128
OrDyFpBnc
ARECIBO OBSERVATORY
BY : BILL SISK
FILE : VMERI14.SCH
Title
VME RADAR INTERFACE
Size B
Document Number
RI2 TEST PAT GEN & 16 BIT PACKER
REV 0
Date: December 16, 1993 Sheet 4 of 4



FORMAT DECODER TABLE

FORMAT	P2 P1 P0	COUNTER PRESET	DCBA	CYCLE LENGTH
16 BIT	000	0	0000	1
8 BIT	001	1	0001	2
4 BIT	010	3	0011	4
2 BIT	011	7	0111	8
1 BIT	111	15	1111	16

LOGIC EQTN'S

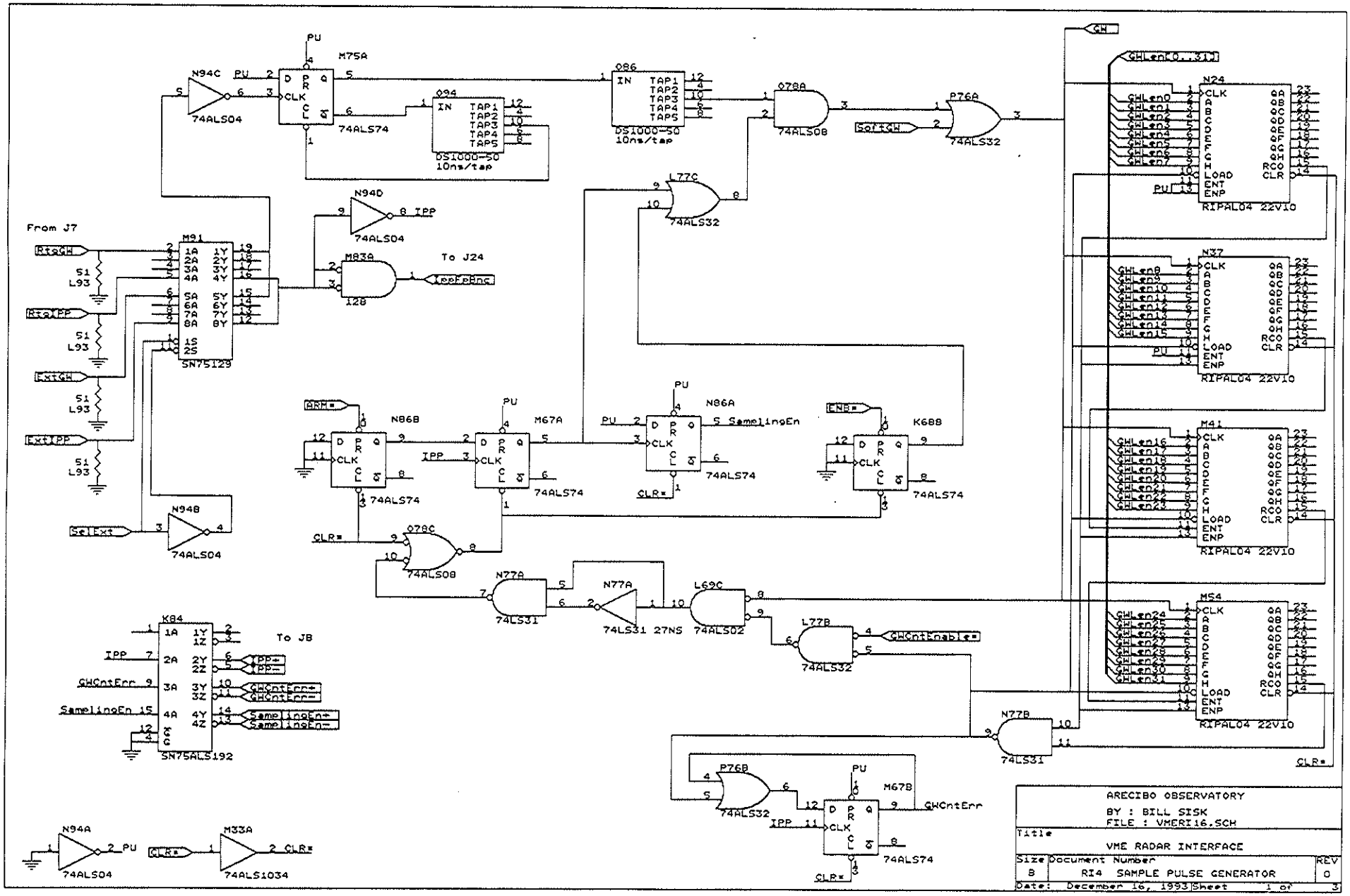
A = P2 + P1 + P1
B = P1
C = P1 * P0
D = P2

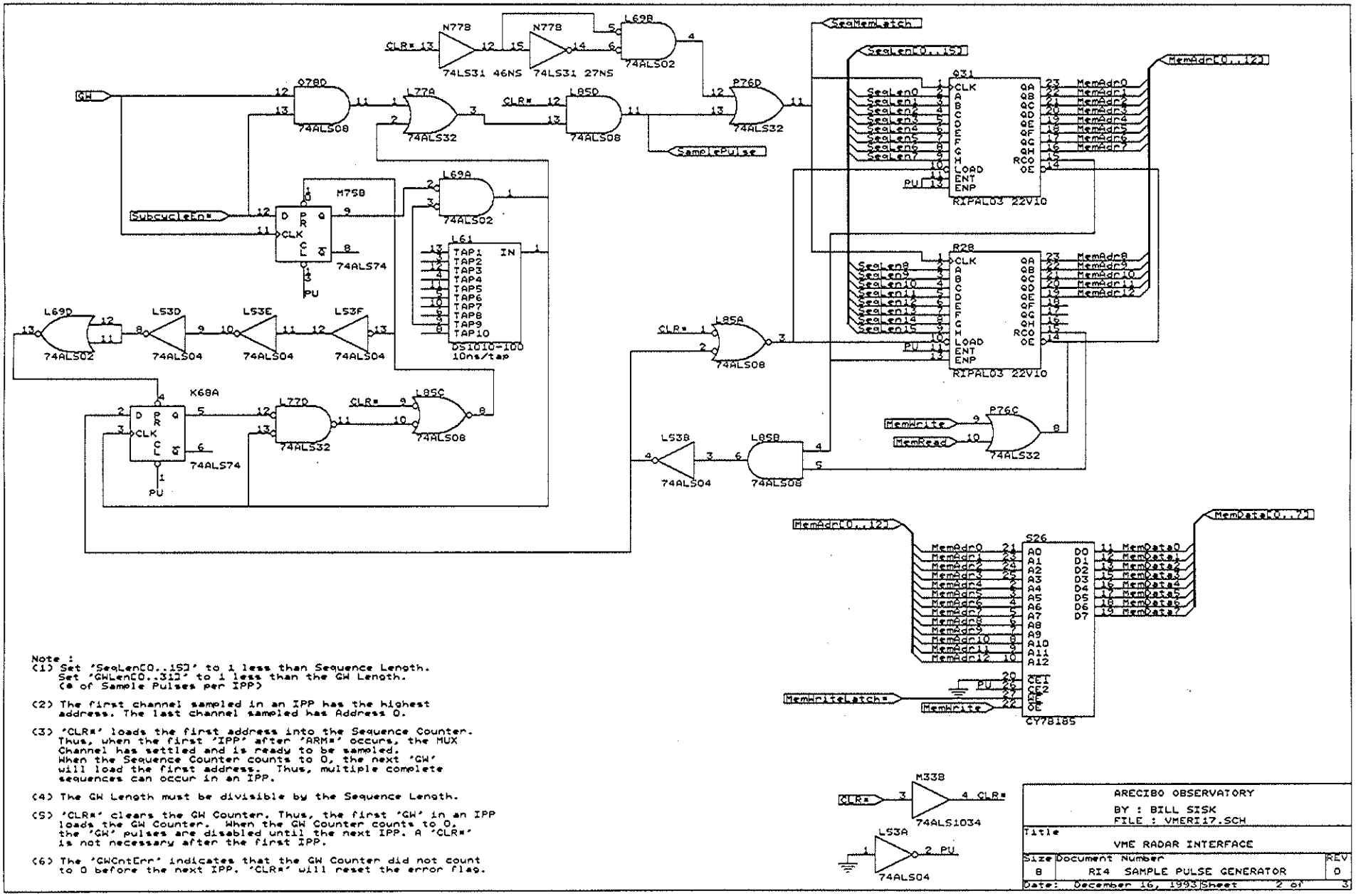
ARECIBO OBSERVATORY
BY : BILL SISK
FILE : VMERI15.SCH

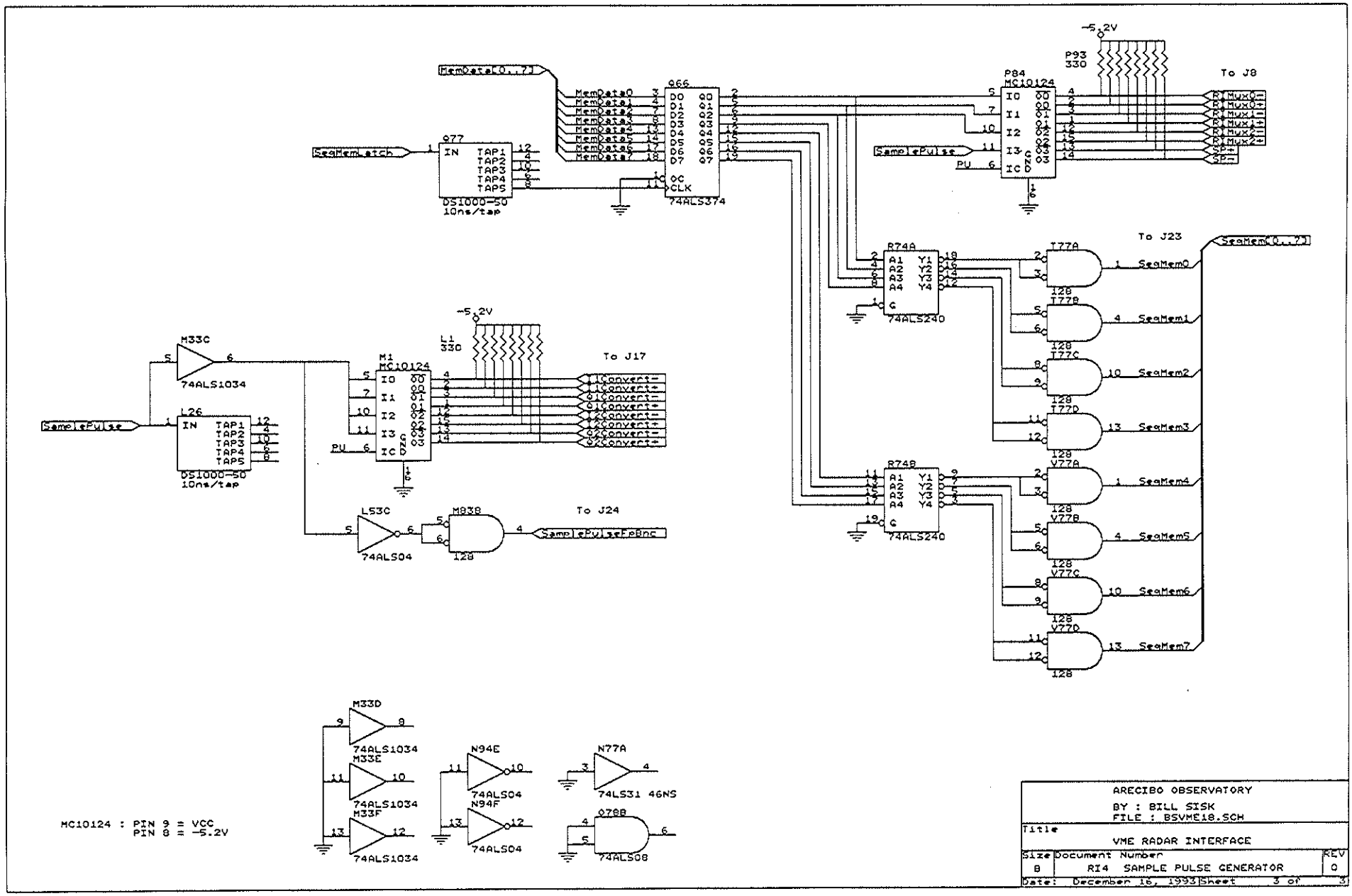
Title
VME RADAR INTERFACE

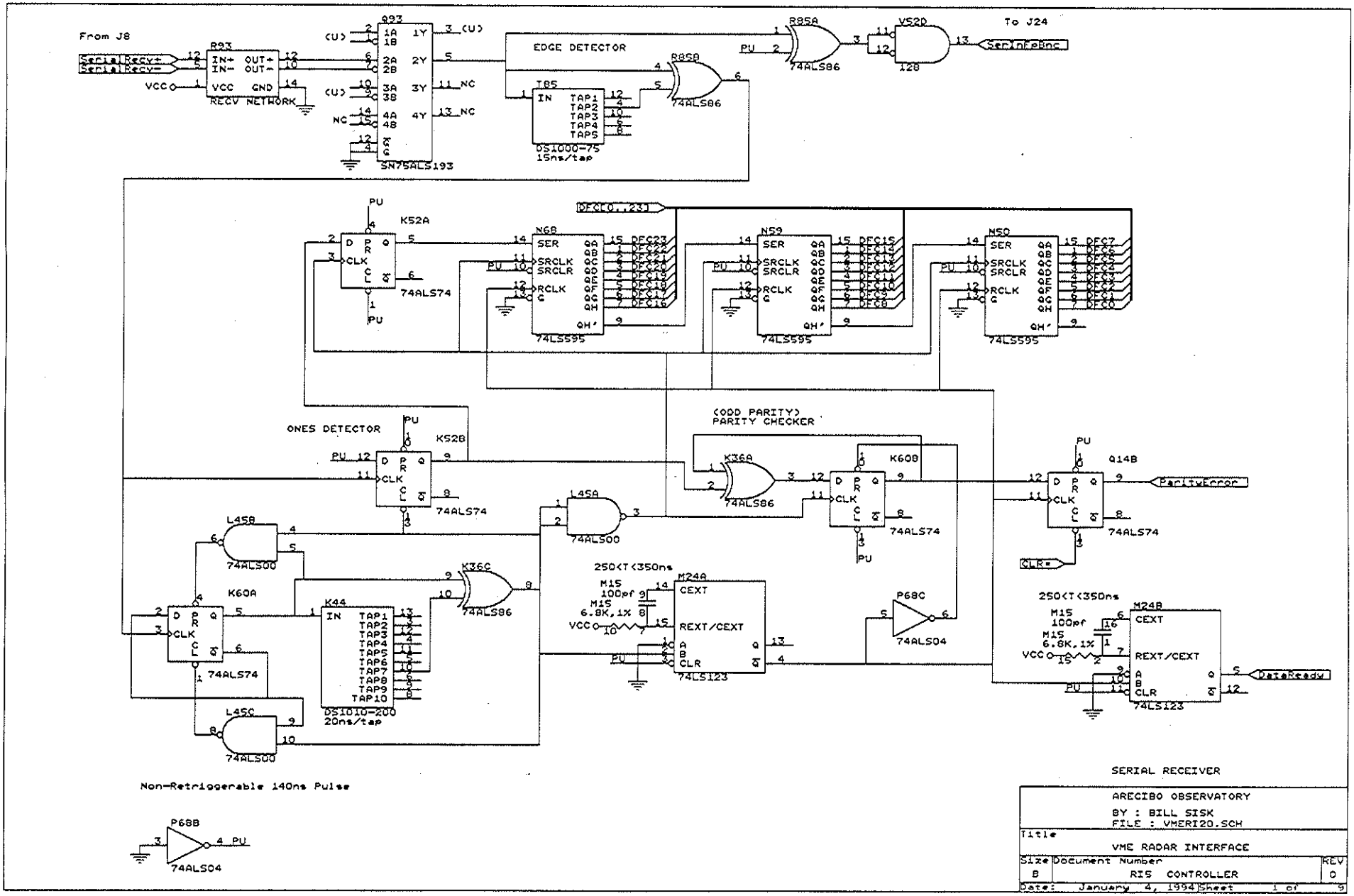
Size: B | Document Number: RI3 INPUT CLOCK GENERATOR | REV:

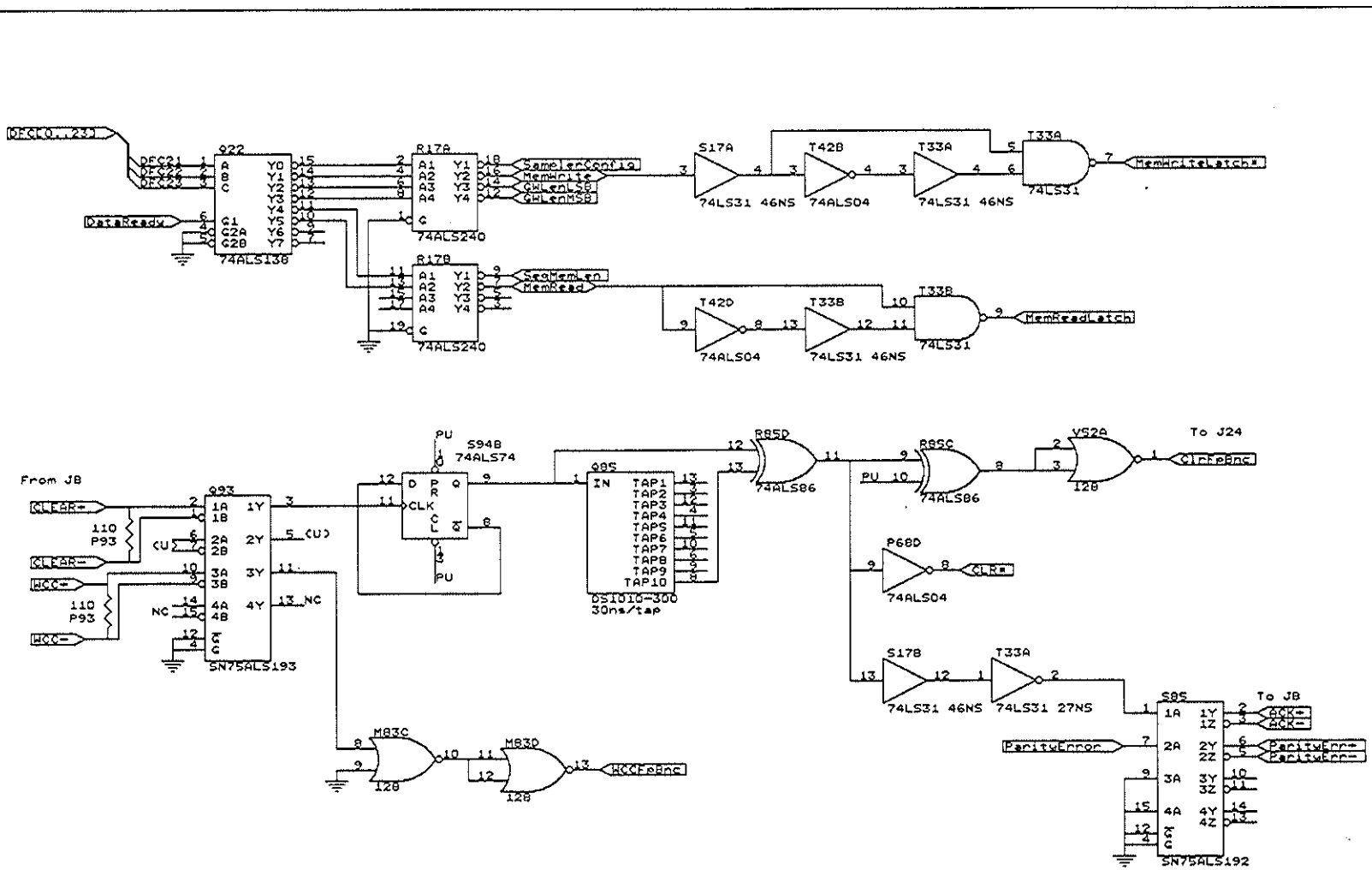
Date: December 16, 1993 | Sheet 1 of 1

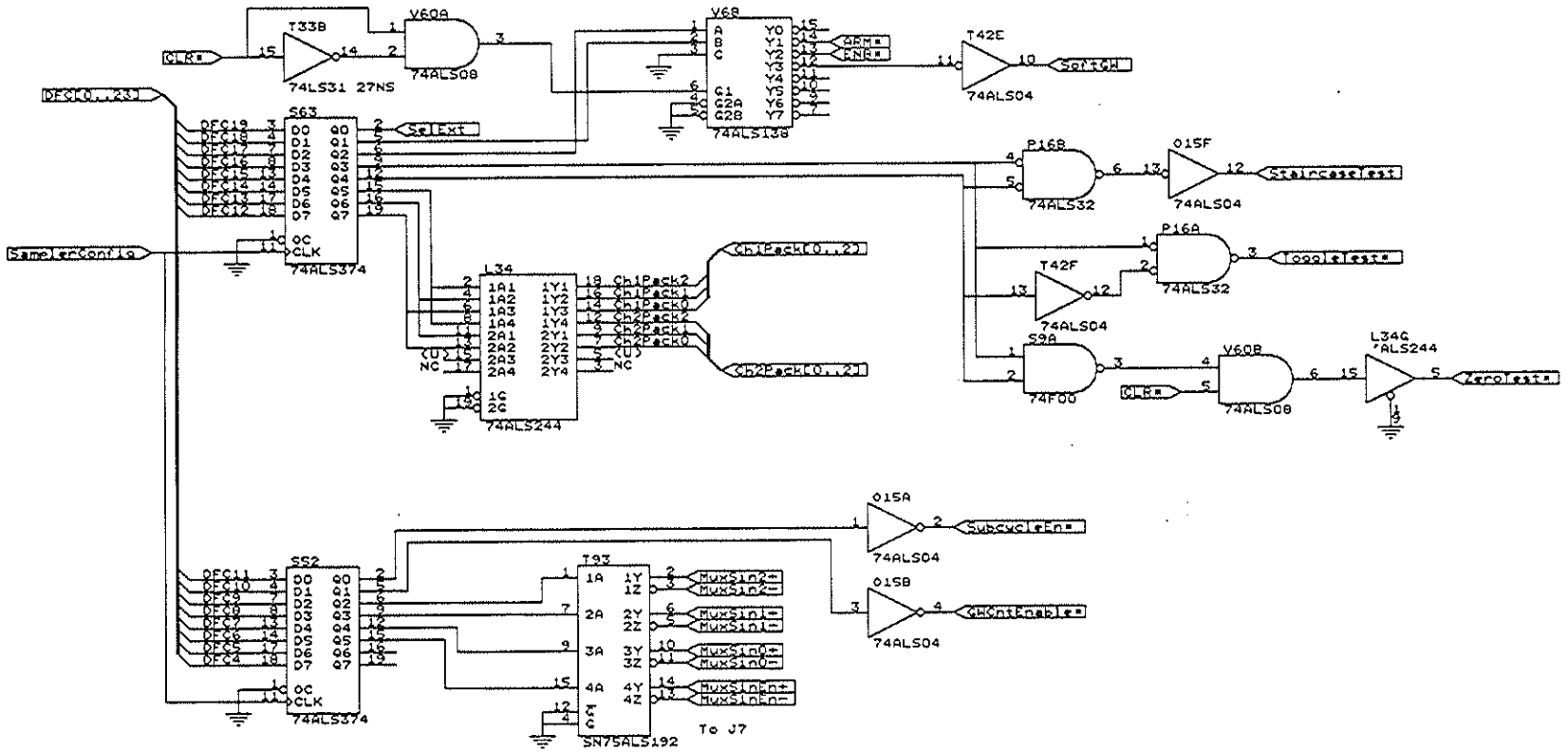

PU
M75A
N94C
74ALS04
74ALS74
Q94
IN
TAP1
TAP2
TAP3
TAP4
TAP5
DS1000-50
10ns/tap
Q86
DS1000-50
10ns/tap
Q78A
74ALS08
P76A
74ALS32
SoftGH
GH
GHLen[0..31]
N24
CLK
LOAD
ENT
ENP
RCO
CLR
RIPAL04 22V10
N37
M41
M54
L77C
74ALS32
N94D
74ALS04
IPP
From J7
M91
SN75I29
RtGH
RtIPP
ExtGH
ExtIPP
S1
L93
M83A
128
To J24
ExtIpBnc
SelExt
N94B
74ALS04
ARM*
N86B
M67A
N86A
SamplingEn
K68B
ENB*
74ALS74
CLR*
Q78C
74ALS08
N77A
74LS31
74LS31 27NS
L69C
74ALS02
L77B
74ALS32
GHCntEnable*
N77B
74LS31
K84
SN75ALS192
To JB
GHCntErr
SamplingEn
P76B
74ALS32
M67B
GHCntErr
N94A
74ALS04
M33A
74ALS1034
CLR*
ARECIBO OBSERVATORY
BY : BILL SISK
FILE : VMERI16.SCH
Title
VME RADAR INTERFACE
Size
B
Document Number
RI4 SAMPLE PULSE GENERATOR
REV
0
Date: December 16, 1993
Sheet 1 of 3


N77B
74LS31 46NS
N77B
74LS31 27NS
L69B
74ALS02
CLR*
SeqMemLatch
SeqLen[0..15]
MemAdr[0..12]
Q78D
74ALS08
L77A
74ALS32
L85D
74ALS08
P76D
74ALS32
SamplePulse
GW
Q31
RIPAL03 22V10
SeqLen0
SeqLen1
SeqLen2
SeqLen3
SeqLen4
SeqLen5
SeqLen6
SeqLen7
MemAdr0
MemAdr1
MemAdr2
MemAdr3
MemAdr4
MemAdr5
MemAdr6
MemAdr7
PU
LOAD
ENT
ENP
RCO
OE
M75B
74ALS74
SwpCycleEn*
L69A
74ALS02
L61
DS1010-100
10ns/tap
TAP1
TAP2
TAP3
TAP4
TAP5
TAP6
TAP7
TAP8
TAP9
TAP10
IN
R28
SeqLen8
SeqLen9
SeqLen10
SeqLen11
SeqLen12
SeqLen13
SeqLen14
SeqLen15
MemAdr8
MemAdr9
MemAdr10
MemAdr11
MemAdr12
L69D
74ALS02
L53D
74ALS04
L53E
74ALS04
L53F
74ALS04
L85A
74ALS08
K68A
74ALS74
L77D
74ALS32
L85C
74ALS08
L53B
74ALS04
L85B
74ALS08
MemWrite
MemRead
P76C
74ALS32
MemAdr[0..12]
MemData[0..7]
S26
CY7B185
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
D0
D1
D2
D3
D4
D5
D6
D7
CE1
CE2
OE
MemWriteLatch*
M33B
74ALS1034
CLR*
L53A
74ALS04
PU
Note :
(1) Set 'SeqLen[0..15]' to 1 less than Sequence Length.
Set 'GWLen[0..31]' to 1 less than the GW Length.
(# of Sample Pulses per IPP)
(2) The first channel sampled in an IPP has the highest address. The last channel sampled has Address 0.
(3) 'CLR*' loads the first address into the Sequence Counter. Thus, when the first 'IPP' after 'ARM*' occurs, the MUX Channel has settled and is ready to be sampled. When the Sequence Counter counts to 0, the next 'GW' will load the first address. Thus, multiple complete sequences can occur in an IPP.
(4) The GW Length must be divisible by the Sequence Length.
(5) 'CLR*' clears the GW Counter. Thus, the first 'GW' in an IPP loads the GW Counter. When the GW Counter counts to 0, the 'GW' pulses are disabled until the next IPP. A 'CLR*' is not necessary after the first IPP.
(6) The 'GWCntErr' indicates that the GW Counter did not count to 0 before the next IPP. 'CLR*' will reset the error flag.
ARECIBO OBSERVATORY
BY : BILL SISK
FILE : VMERI17.SCH
Title
VME RADAR INTERFACE
Size
B
Document Number
RI4 SAMPLE PULSE GENERATOR
REV
0
Date: December 16, 1993 Sheet 2 of 3


MemData[0..7]
SeqMemLatch
977
IN
TAP1
TAP2
TAP3
TAP4
TAP5
DS1000-50
10ns/tap
966
D0 Q0
D1 Q1
D2 Q2
D3 Q3
D4 Q4
D5 Q5
D6 Q6
D7 Q7
OC
CLK
74ALS374
-5.2V
P93
330
P84
MC10124
I0
I1
I2
I3
IC
SampleFulse
PU
To J8
R74A
R74B
A1 Y1
A2 Y2
A3 Y3
A4 Y4
G
74ALS240
To J23
SeqMem[0..7]
T77A
T77B
T77C
T77D
V77A
V77B
V77C
V77D
I28
SeqMem0
SeqMem1
SeqMem2
SeqMem3
SeqMem4
SeqMem5
SeqMem6
SeqMem7
M33C
74ALS1034
L26
M1
L1
330
To J17
Convert+
Convert-
L53C
74ALS04
M93B
To J24
SampleFulseToBnc
M33D
M33E
M33F
N94E
N94F
N77A
74LS31 46NS
Q70B
74ALS08
MC10124 : PIN 9 = VCC
PIN 8 = -5.2V
ARECIBO OBSERVATORY
BY : BILL SISK
FILE : BSVME18.SCH
Title
VME RADAR INTERFACE
Size
B
Document Number
RI4 SAMPLE PULSE GENERATOR
REV
0
Date: December 16, 1993
Sheet 3 of 3

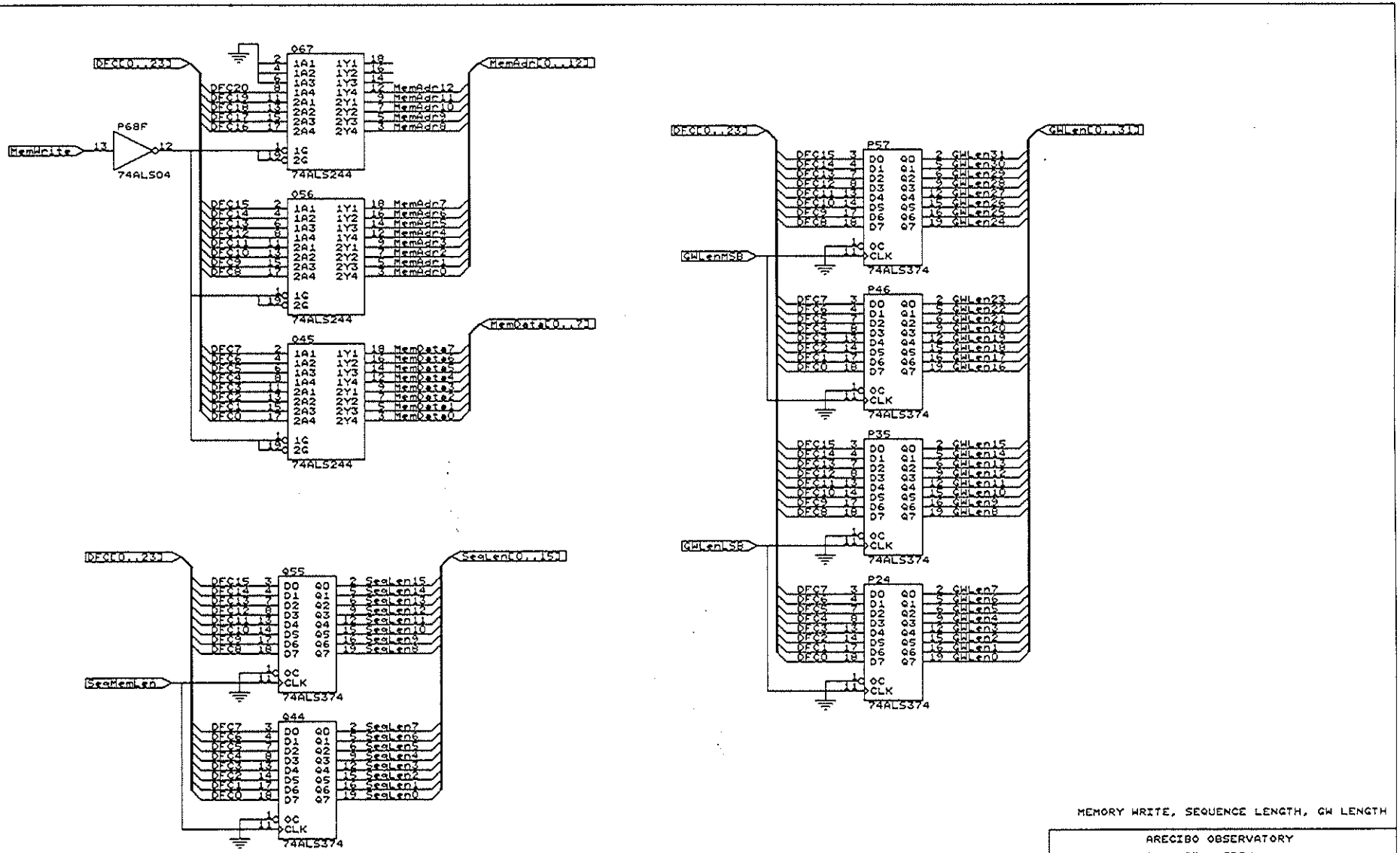

From J8
SerialRecv+
SerialRecv-
VCC
R93
RECV NETWORK
Q93
SN75ALS193
EDGE DETECTOR
T85
DS1000-75
15ns/tap
R85A
R85B
74ALS86
V52D
128
To J24
SerInFoBnc
PU
K52A
74ALS74
N68
N59
N50
74LS595
DFC(0..23)
ONES DETECTOR
K52B
(ODD PARITY)
PARITY CHECKER
K36A
K60B
Q14B
ParityError
CLR*
L45A
74ALS00
L45B
L45C
K60A
K44
DS1010-200
20ns/tap
K36C
250<T<350ns
M15
100pf
M15
6.8K,1%
VCC
M24A
M24B
CEXT
REXT/CEXT
74LS123
P68C
74ALS04
DataReady
Non-Retriggerable 140ns Pulse
P68B
SERIAL RECEIVER
ARECIBO OBSERVATORY
BY : BILL SISK
FILE : VMERI20.SCH
Title
VME RADAR INTERFACE
Size
B
Document Number
RIS CONTROLLER
REV
0
Date: January 4, 1994
Sheet 1 of 9

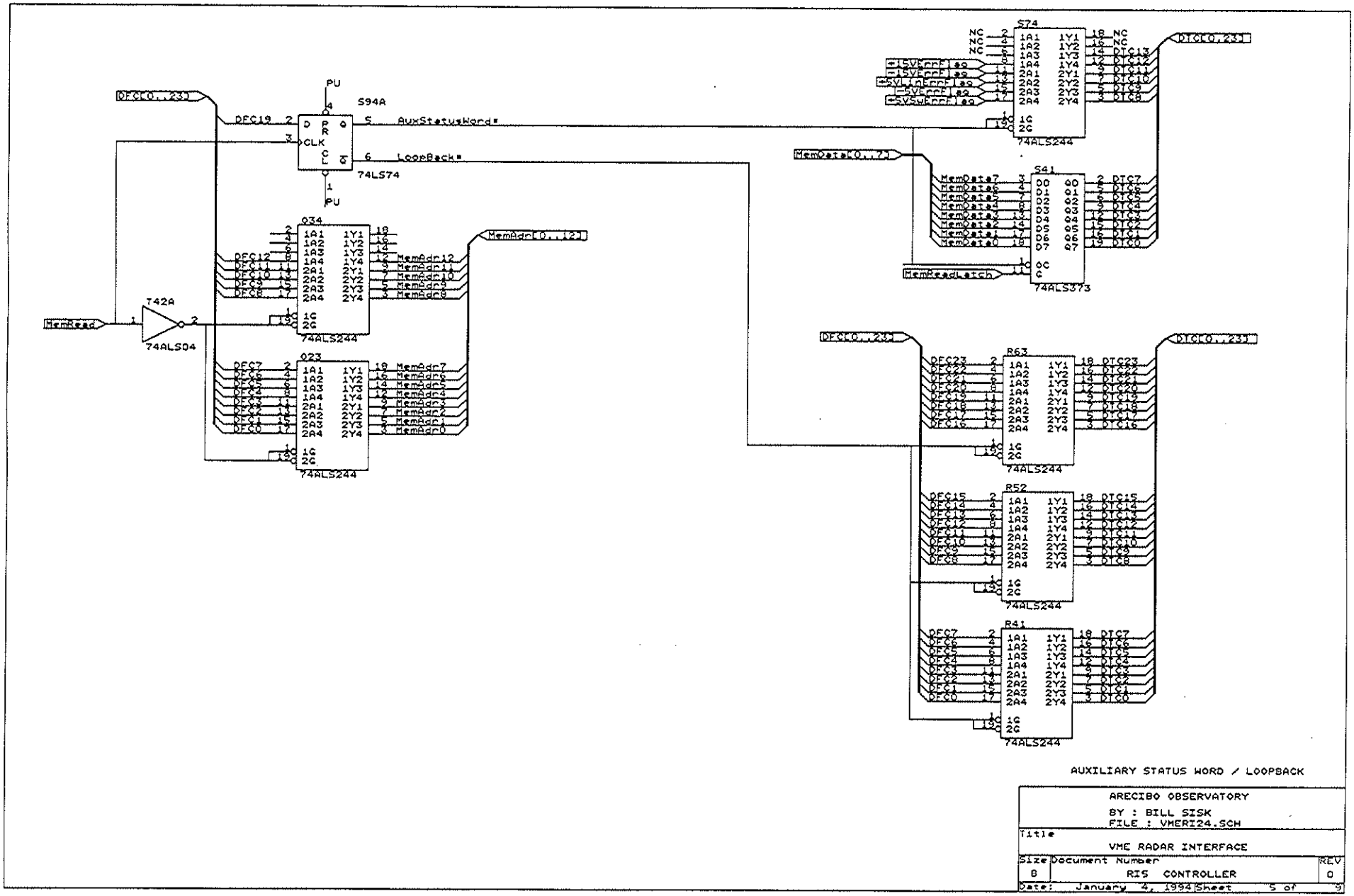

DFC[0..23]
Q22
74ALS138
DataReady
R17A
74ALS240
SamplerConfig
MemWrite
GHLenLSB
GHLenMSB
S17A
74LS31 46NS
T42B
74ALS04
T33A
74LS31 46NS
T33A
74LS31
MemWriteLatch*
R17B
74ALS240
SeqMemEn
MemRead
T42D
74ALS04
T33B
74LS31 46NS
T33B
74LS31
MemReadLatch
From JB
Q93
SN75ALS193
CLEAR-
WCC-
110
P93
(U)
NC
S94B
74ALS74
PU
Q9S
DS1010-300
30ns/tap
TAP1
TAP2
TAP3
TAP4
TAP5
TAP6
TAP7
TAP8
TAP9
TAP10
R85D
74ALS86
R85C
74ALS86
V52A
128
To J24
ClrFeBnc
P68D
74ALS04
CLR*
S17B
74LS31 46NS
T33A
74LS31 27NS
S8S
SN75ALS192
To JB
ParityError
M83C
128
M83D
128
WCCFeBnc
P68A
74ALS04
PU-RIS
(U) : Gate is being used in another location.
COMMAND BITS DECODER
ARECIBO OBSERVATORY
BY : BILL SISK
FILE : VMERI21.SCH
Title
VME RADAR INTERFACE
Size B
Document Number
RI5 CONTROLLER
REV 0
Date: January 4, 1994
Sheet 2 of 9



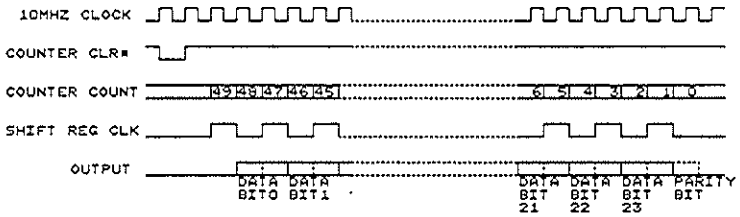
SAMPLER CONFIGURATION WORD DECODER

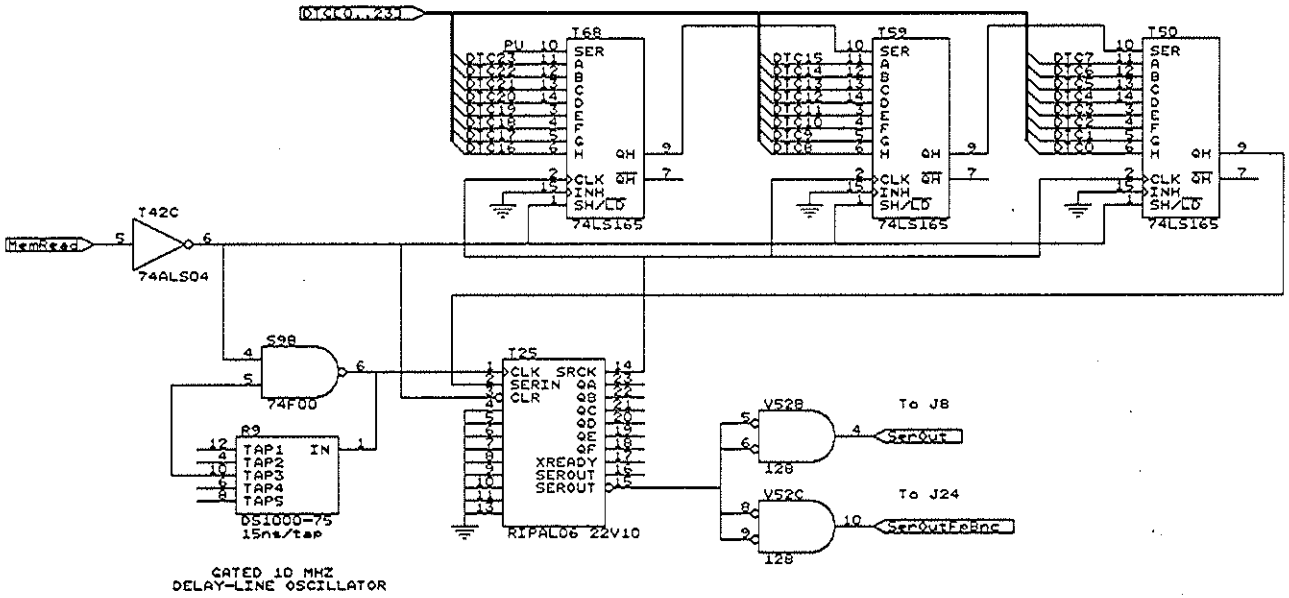
ARECIBO OBSERVATORY BY : BILL SISK FILE : VMERI22.SCH		
Title: VME RADAR INTERFACE		
Size: B	Document Number: RIS CONTROLLER	REV: 0
Date: January 4, 1994	Sheet 3 of 9	


MEMORY WRITE, SEQUENCE LENGTH, GW LENGTH
ARECIBO OBSERVATORY
BY : BILL SISK
FILE : VMERI23.SCH
Title
VME RADAR INTERFACE
Size 8
Document Number
RIS CONTROLLER
REV 0
Date: January 4, 1994 Sheet 4 of 9


S74
74ALS244
S41
74ALS373
S94A
74LS74
T42A
74ALS04
034
74ALS244
023
74ALS244
R63
74ALS244
R52
74ALS244
R41
74ALS244
AUXILIARY STATUS WORD / LOOPBACK
ARECIBO OBSERVATORY
BY : BILL SISK
FILE : VMERI24.SCH
Title
VME RADAR INTERFACE
Size B
Document Number
RIS CONTROLLER
REV 0
Date: January 4, 1994 Sheet 5 of 9

NOTE : Output has a transition at the beginning of each 200ns cell. If the data bit is a 1, there is also a transition at midcell. The number of "1's", including the parity bit will always be odd.(odd parity)

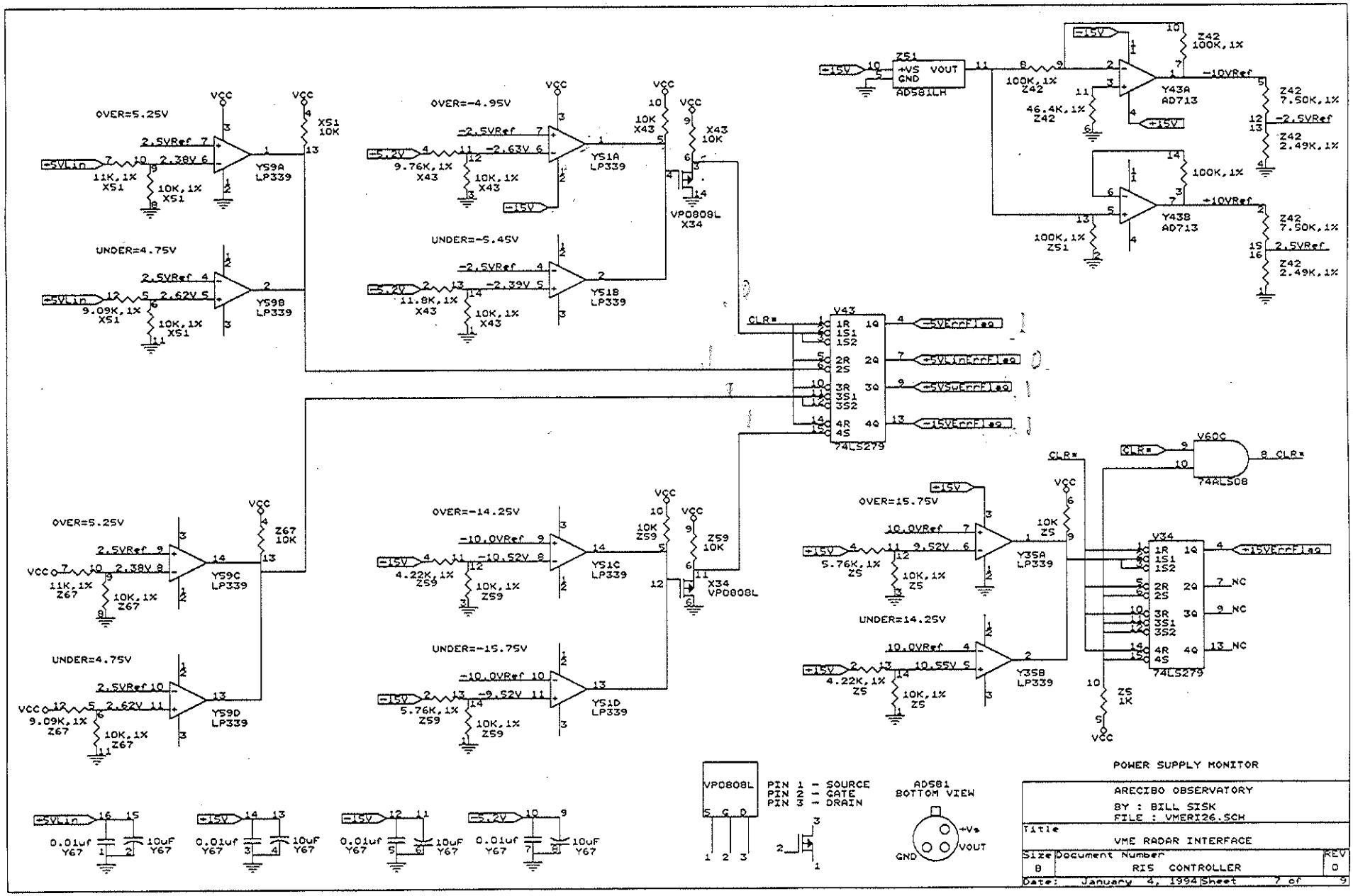


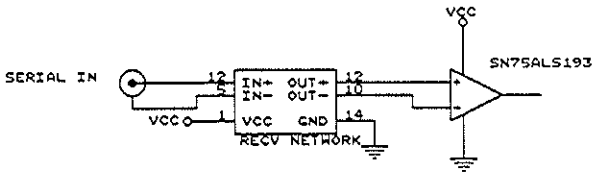


PU-RIS PU

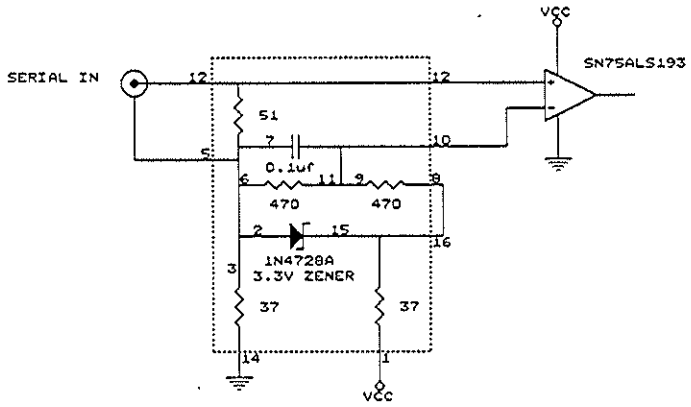
SERIAL TRANSMITTER

ARECIBO OBSERVATORY BY : BILL SISK FILE : VMERI25.SCH		
Title: VME RADAR INTERFACE		
Size: B	Document Number: RIS CONTROLLER	REV: 0
Date: January 4, 1994	Sheet 6 of 9	

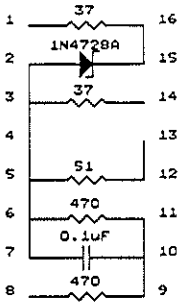

OVER=5.25V
UNDER=4.75V
OVER=-4.95V
UNDER=-5.45V
OVER=-14.25V
UNDER=-15.75V
OVER=15.75V
UNDER=14.25V
AD581LH
74LS279
74LS08
VP0808L
POWER SUPPLY MONITOR
ARECIBO OBSERVATORY
BY : BILL SISK
FILE : VMERI26.SCH
VME RADAR INTERFACE
RIS CONTROLLER
January 4, 1994



A. SCHEMATIC USAGE

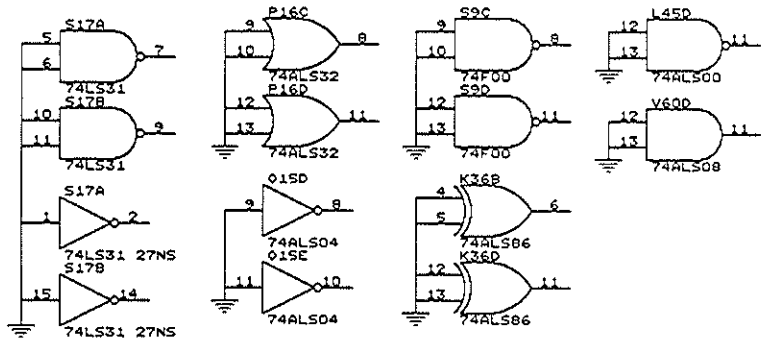


B. DETAILED SCHEMATIC



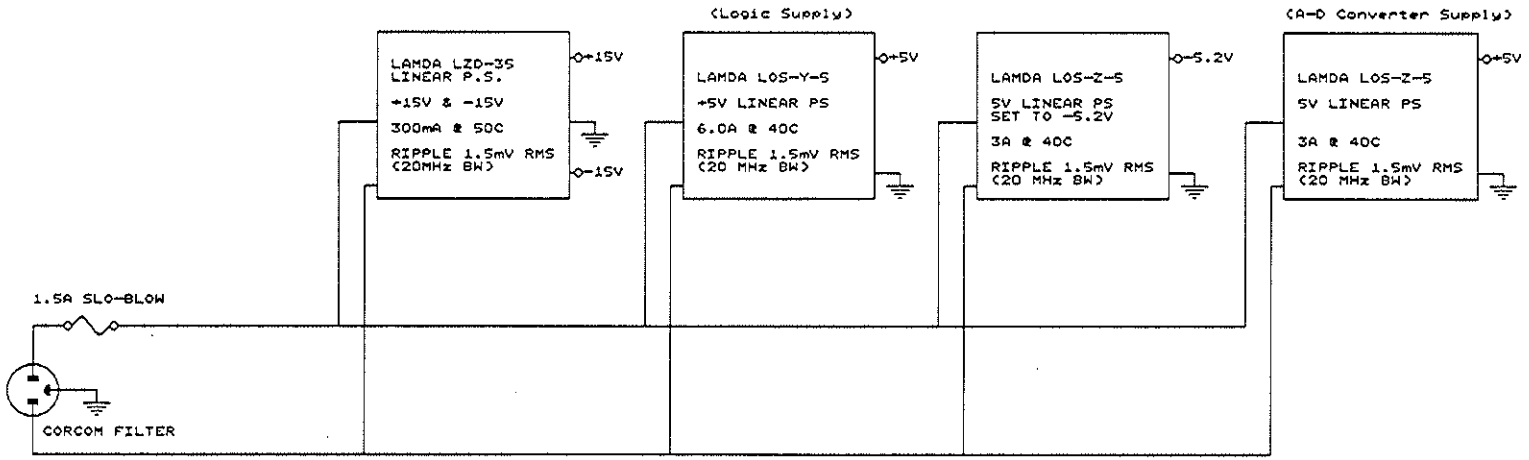
C. DIP CARRIER DETAIL

ARECIBO OBSERVATORY		
BY : BILL SISK FILE : VMERI27.SCH		
Title: VME RADAR INTERFACE		
Size: B	Document Number: RIS CONTROLLER	REV: 0
Date: January 4, 1994	Sheet 8 of 9	

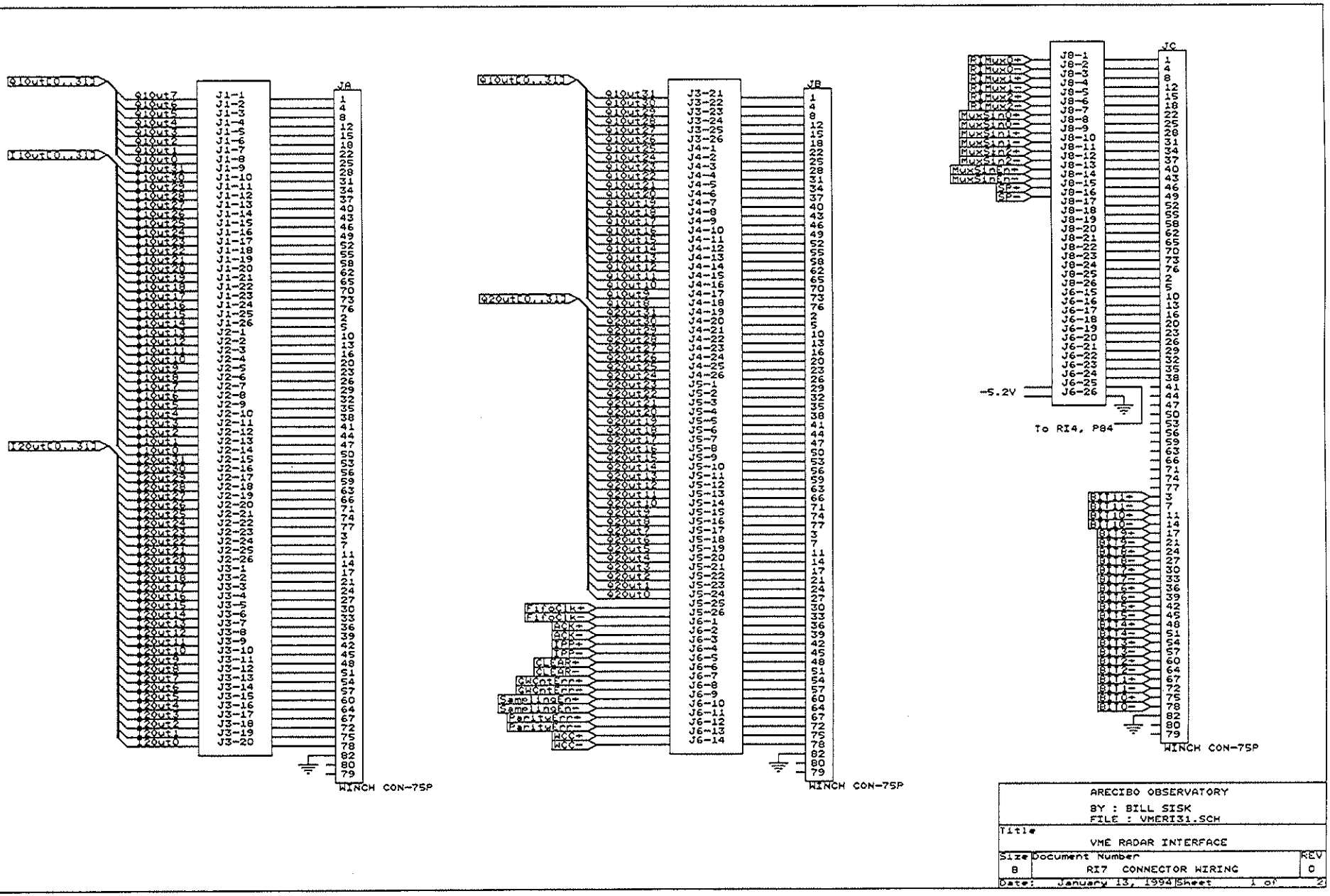


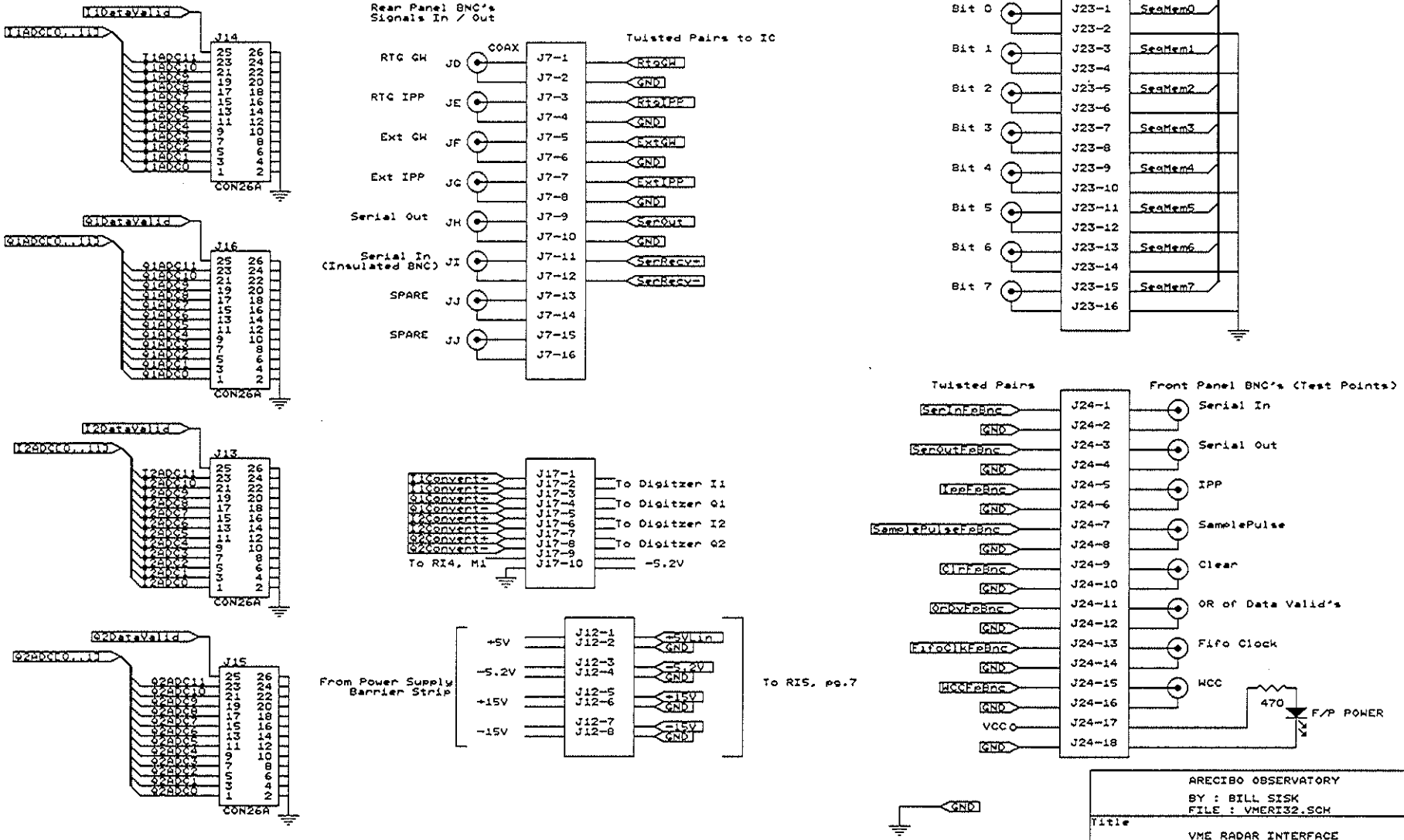
UNUSED GATES

	ARECIBO OBSERVATORY BY : BILL SISK FILE : VMERI28.SCH	
Title	VME RADAR INTERFACE	
Size B	Document Number RIS CONTROLLER	REV 0
Date: January 4, 1994	Sheet 9 of 9	

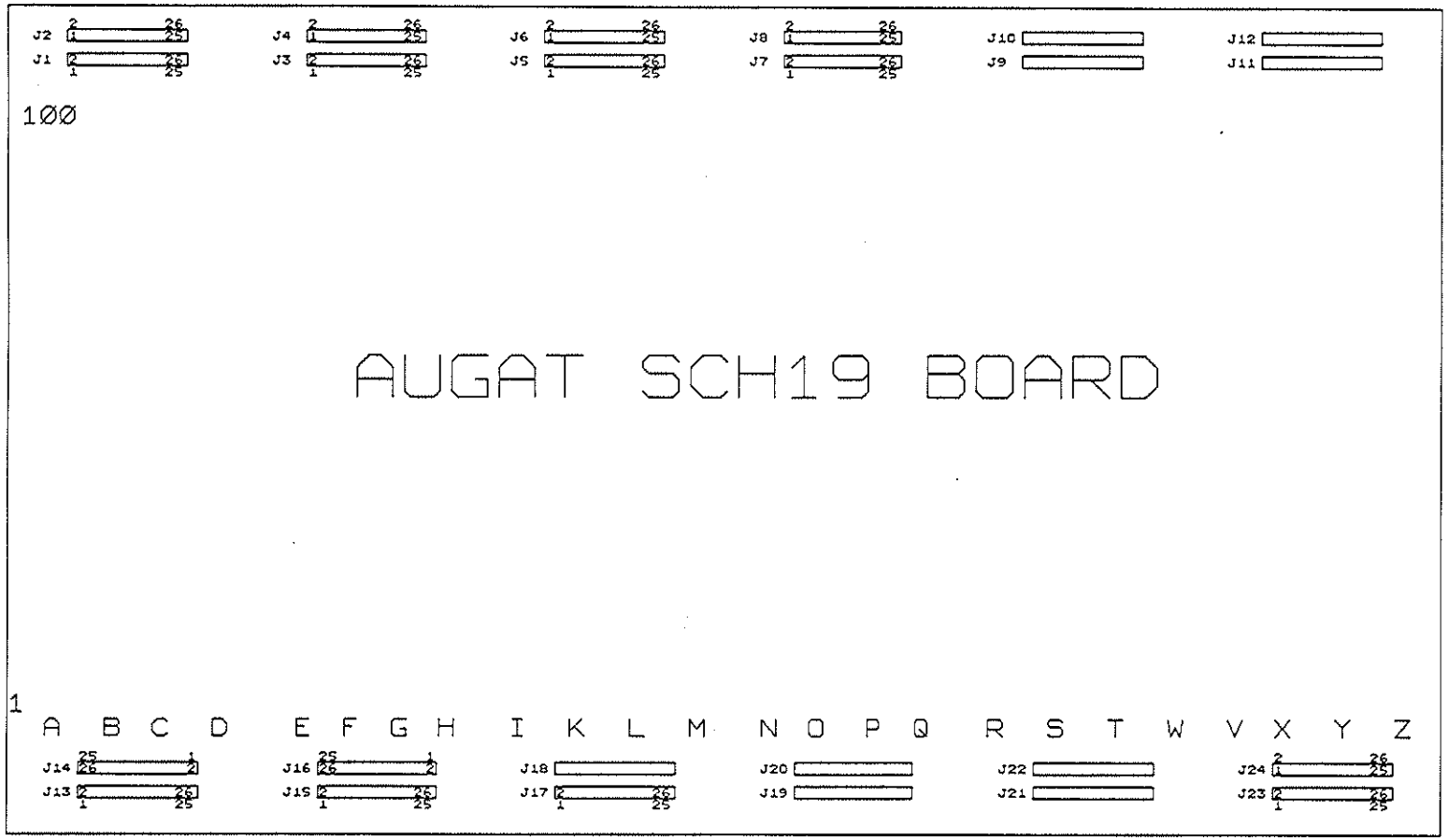


ARECIBO OBSERVATORY	
BY : BILL SISK	
FILE : VMERI3O.SCH	
Title: VME RADAR INTERFACE	
Size: B	Document Number: RI6 POWER SUPPLY — REV: 0
Date: January 4, 1994	Sheet 1 of 1


Q10out[0..31]
I10out[0..31]
I20out[0..31]
Q20out[0..31]
J1
J2
J3
J4
J5
J6
J8
JA
JB
JC
WINCH CON-75P
WINCH CON-75P
WINCH CON-75P
-5.2V
To RI4, P84
ARECIBO OBSERVATORY
BY : BILL SISK
FILE : VMERI31.SCH
Title
VME RADAR INTERFACE
Size
B
Document Number
RI7 CONNECTOR WIRING
REV
0
Date: January 13, 1994
Sheet 1 of 2

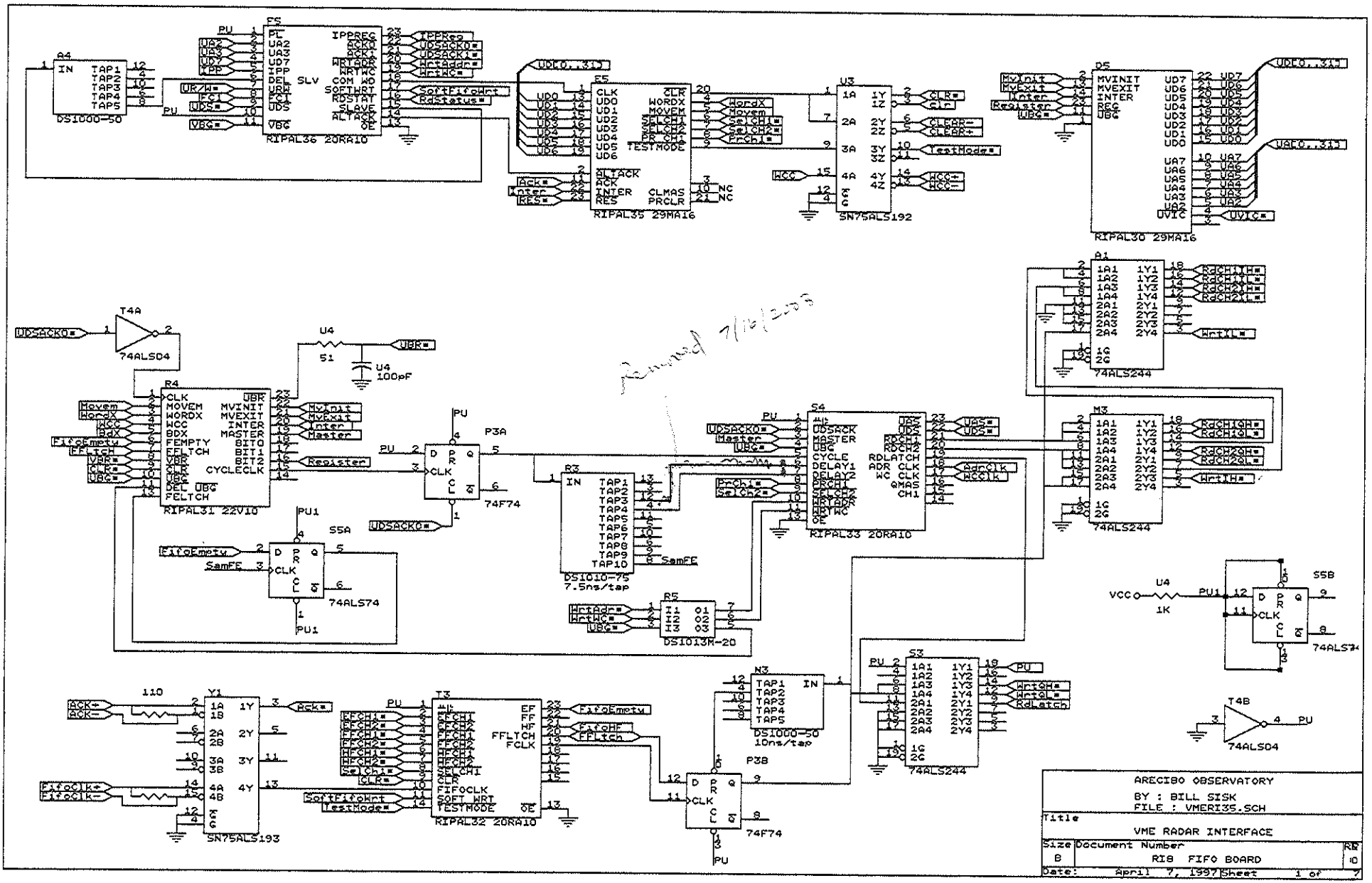

I1DataValid
I1ADC[0..11]
J14
I1ADC11
I1ADC10
I1ADC9
I1ADC8
I1ADC7
I1ADC6
I1ADC5
I1ADC4
I1ADC3
I1ADC2
I1ADC1
I1ADC0
CON26A
Q1DataValid
Q1ADC[0..11]
J16
Q1ADC11
Q1ADC10
Q1ADC9
Q1ADC8
Q1ADC7
Q1ADC6
Q1ADC5
Q1ADC4
Q1ADC3
Q1ADC2
Q1ADC1
Q1ADC0
CON26A
I2DataValid
I2ADC[0..11]
J13
I2ADC11
I2ADC10
I2ADC9
I2ADC8
I2ADC7
I2ADC6
I2ADC5
I2ADC4
I2ADC3
I2ADC2
I2ADC1
I2ADC0
CON26A
Q2DataValid
Q2ADC[0..11]
J15
Q2ADC11
Q2ADC10
Q2ADC9
Q2ADC8
Q2ADC7
Q2ADC6
Q2ADC5
Q2ADC4
Q2ADC3
Q2ADC2
Q2ADC1
Q2ADC0
CON26A
Rear Panel BNC's
Signals In / Out
COAX
Twisted Pairs to IC
RTG CK
JD
RTG IPP
JE
Ext CK
JF
Ext IPP
JG
Serial Out
JH
Serial In
(Insulated BNC)
JI
SPARE
JJ
SPARE
JJ
J7-1
J7-2
J7-3
J7-4
J7-5
J7-6
J7-7
J7-8
J7-9
J7-10
J7-11
J7-12
J7-13
J7-14
J7-15
J7-16
RtgCK
GND
RtgIPP
GND
ExtCK
GND
ExtIPP
GND
SerOut
GND
SerRecv-
SerRecv-
Mux Channel Sequence Bits
Twisted Pairs
SeqMem[0..7]
Bit 0
Bit 1
Bit 2
Bit 3
Bit 4
Bit 5
Bit 6
Bit 7
J23-1
J23-2
J23-3
J23-4
J23-5
J23-6
J23-7
J23-8
J23-9
J23-10
J23-11
J23-12
J23-13
J23-14
J23-15
J23-16
SeqMem0
SeqMem1
SeqMem2
SeqMem3
SeqMem4
SeqMem5
SeqMem6
SeqMem7
I1Convert+
I1Convert-
Q1Convert+
Q1Convert-
I2Convert+
I2Convert-
Q2Convert+
Q2Convert-
To RI4, M1
J17-1
J17-2
J17-3
J17-4
J17-5
J17-6
J17-7
J17-8
J17-9
J17-10
To Digitzer I1
To Digitzer Q1
To Digitzer I2
To Digitzer Q2
-5.2V
From Power Supply
Barrier Strip
+5V
-5.2V
+15V
-15V
J12-1
J12-2
J12-3
J12-4
J12-5
J12-6
J12-7
J12-8
-5V in
GND
-5.2V
GND
+15V
GND
-15V
GND
To RI5, pg.7
Twisted Pairs
Front Panel BNC's (Test Points)
SerInFpBnc
SerOutFpBnc
IppFpBnc
SamplePulseFpBnc
ClrFpBnc
OrDvFpBnc
FifoClkFpBnc
HCCFpBnc
VCC
GND
J24-1
J24-2
J24-3
J24-4
J24-5
J24-6
J24-7
J24-8
J24-9
J24-10
J24-11
J24-12
J24-13
J24-14
J24-15
J24-16
J24-17
J24-18
Serial In
Serial Out
IPP
SamplePulse
Clear
OR of Data Valid's
Fifo Clock
HCC
470
F/P POWER
GND
ARECIBO OBSERVATORY
BY : BILL SISK
FILE : VMERI32.SCH
Title
VME RADAR INTERFACE
Size
B
Document Number
RI7 CONNECTOR WIRING
REV
0
Date: January 4, 1994
Sheet 2 of 2

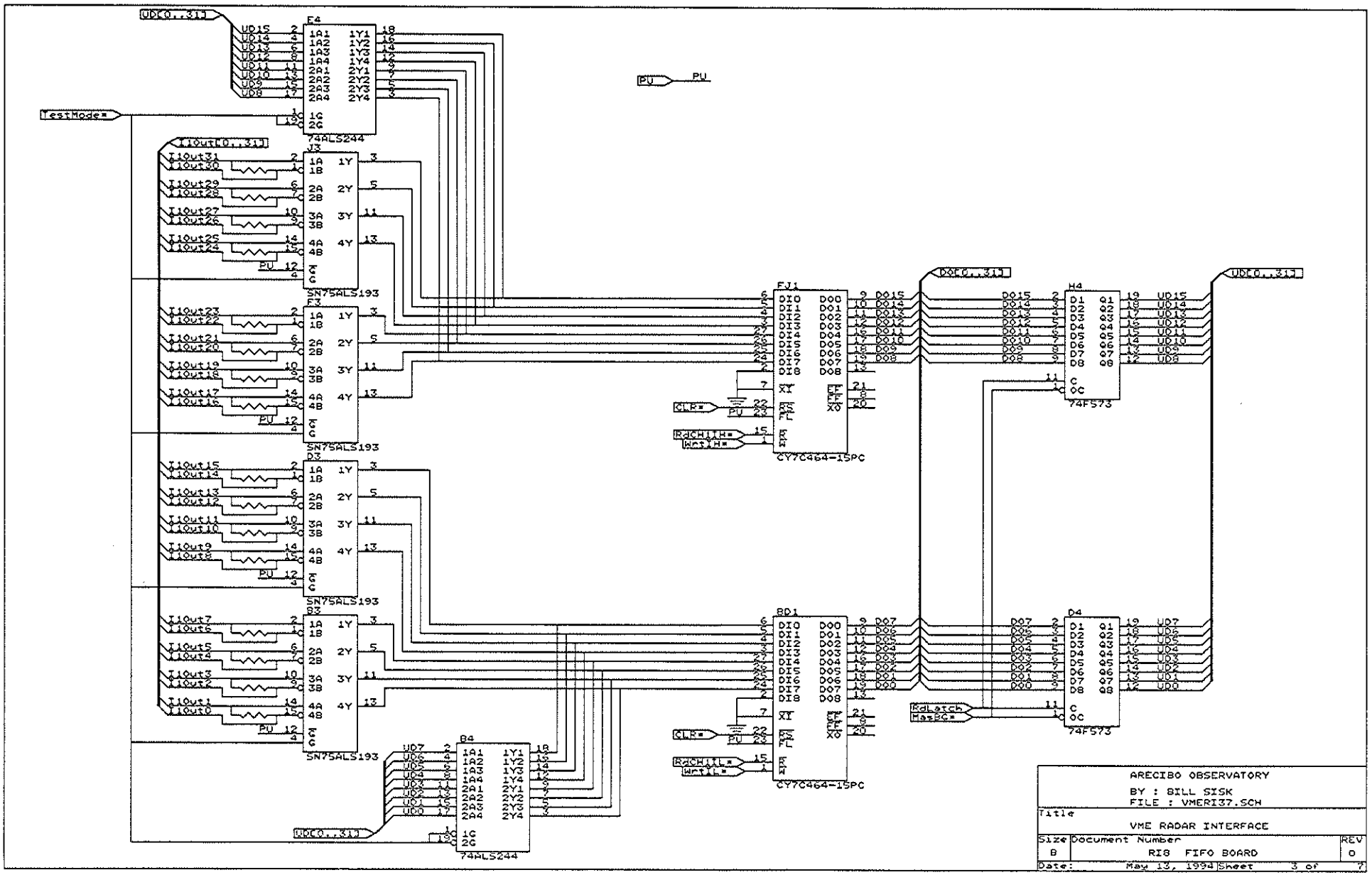
REAR

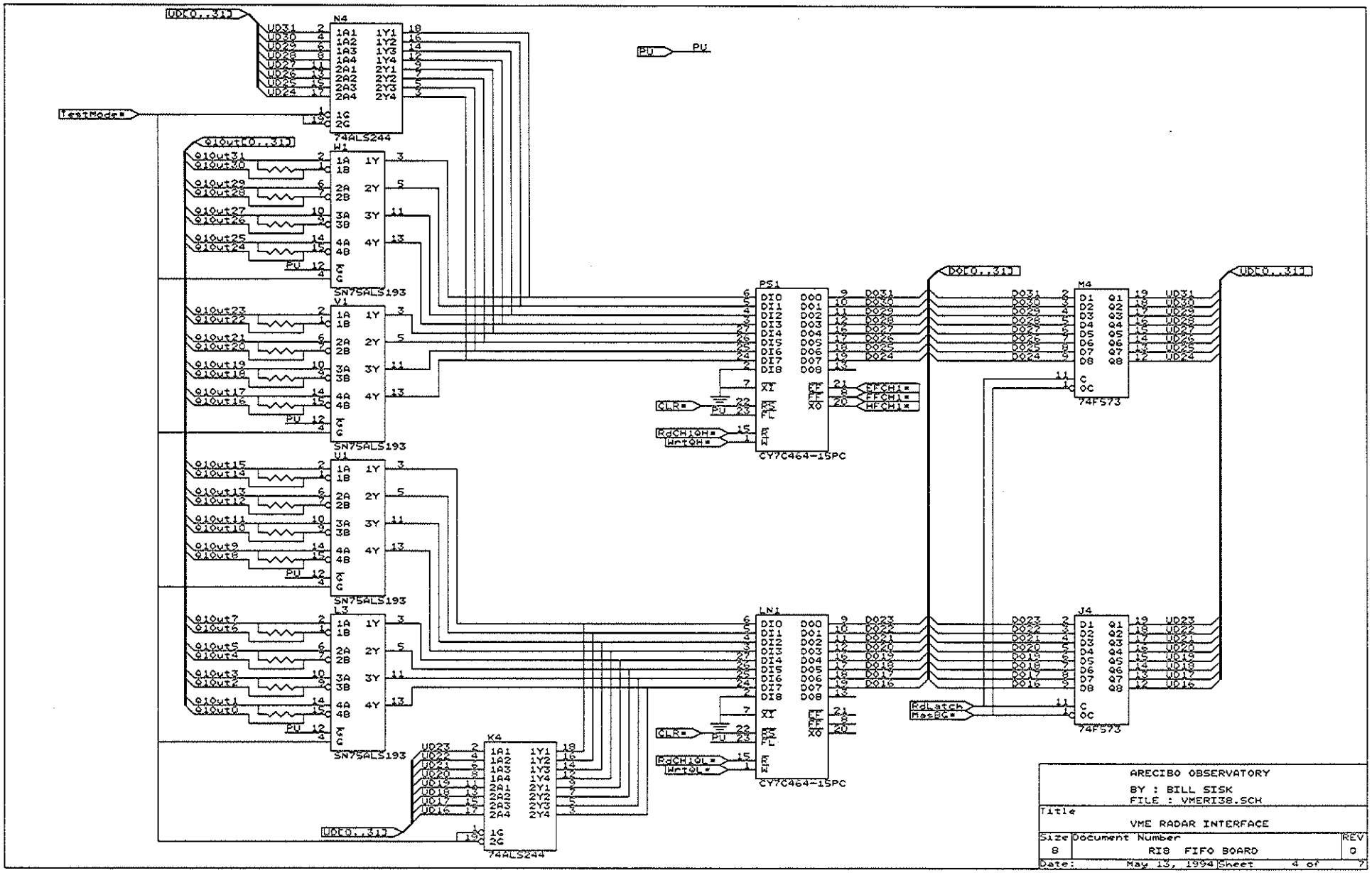


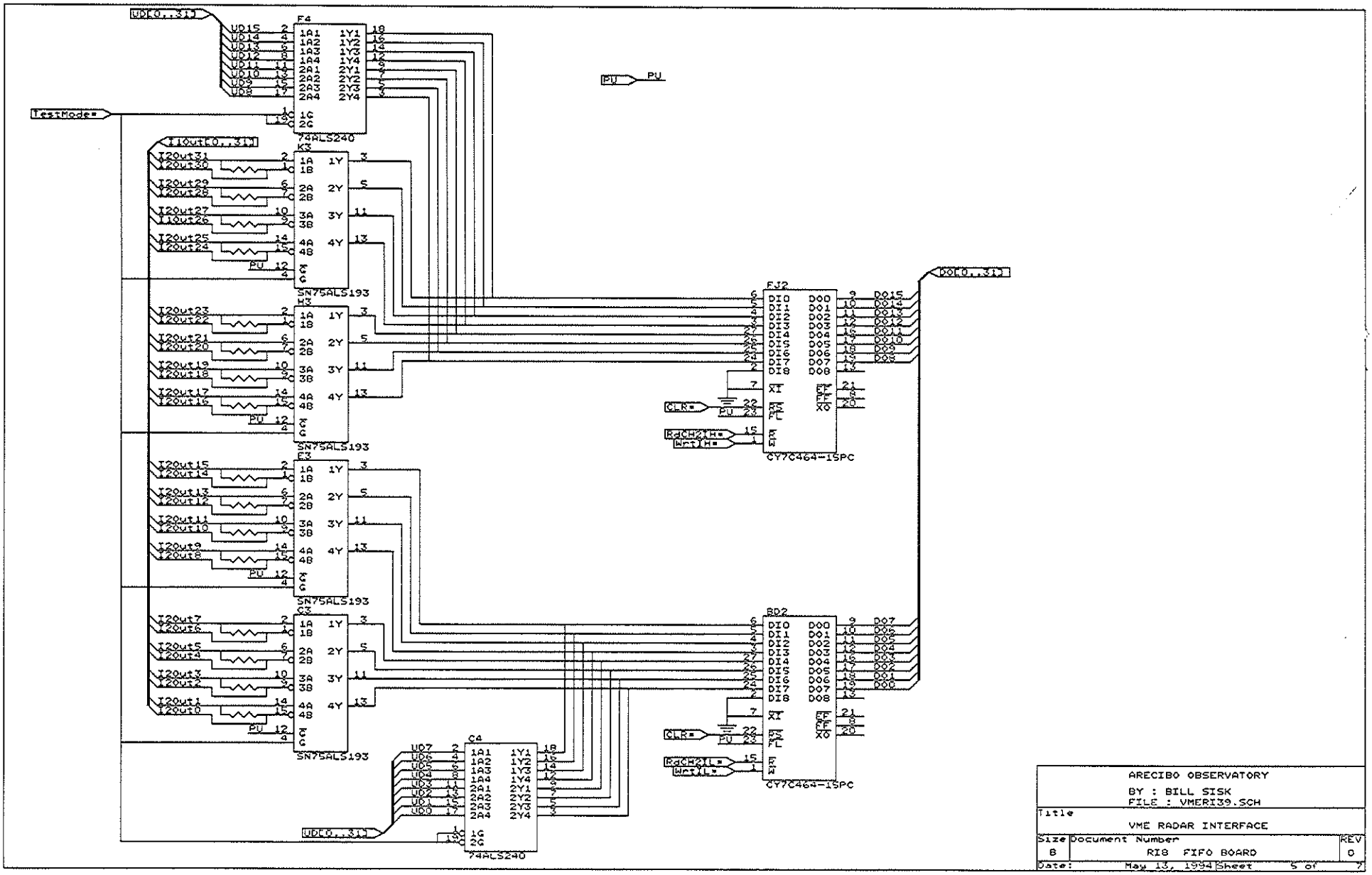
FRONT

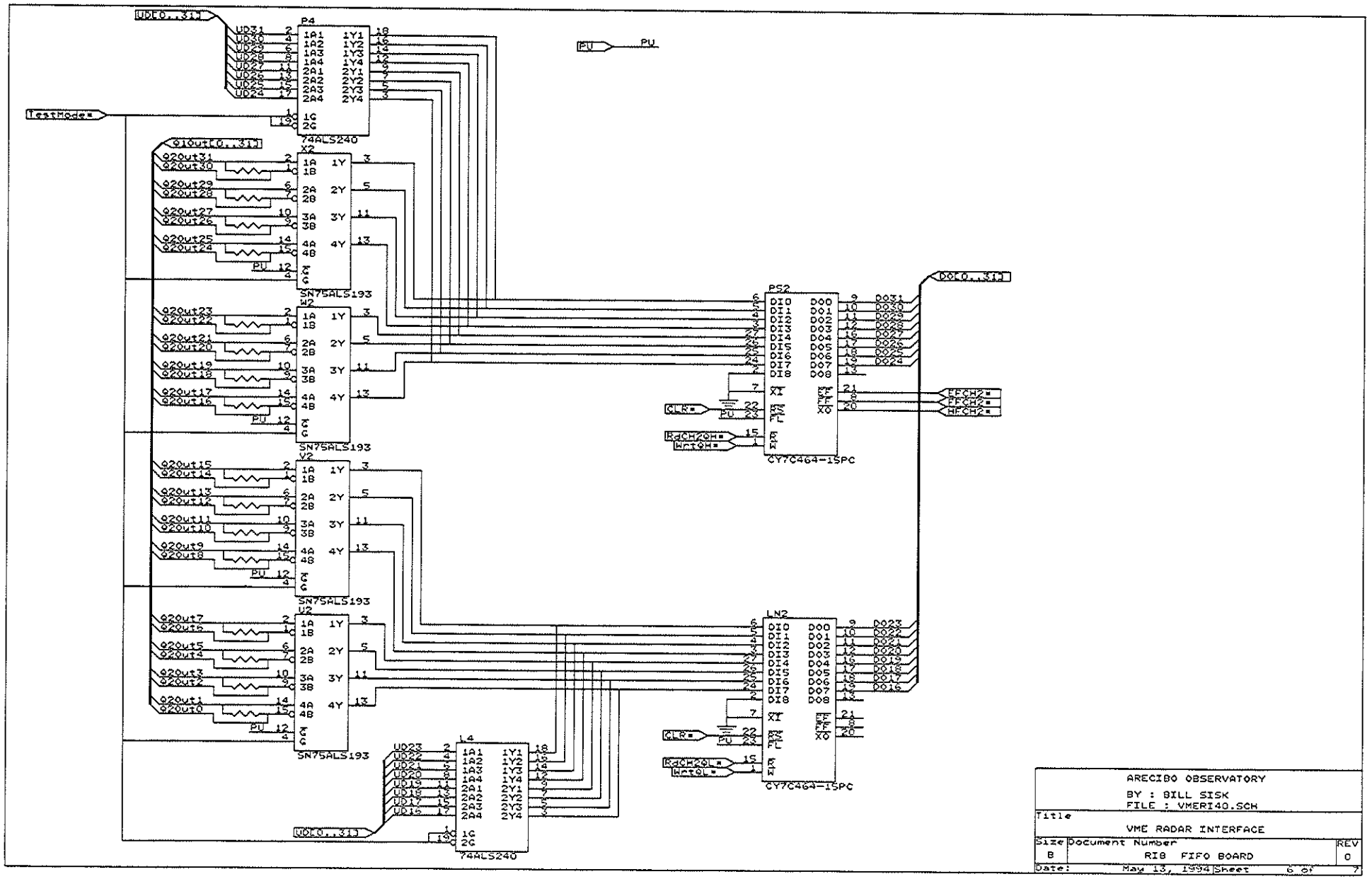
ARECIBO OBSERVATORY		
BY : BILL SISK FILE : VMERI33.SCH		
Title: VME RADAR INTERFACE		
Size: B	Document Number: AUGAT SCH19 BOARD LAYOUT	REV: 0
Date: January 4, 1994	Sheet of	

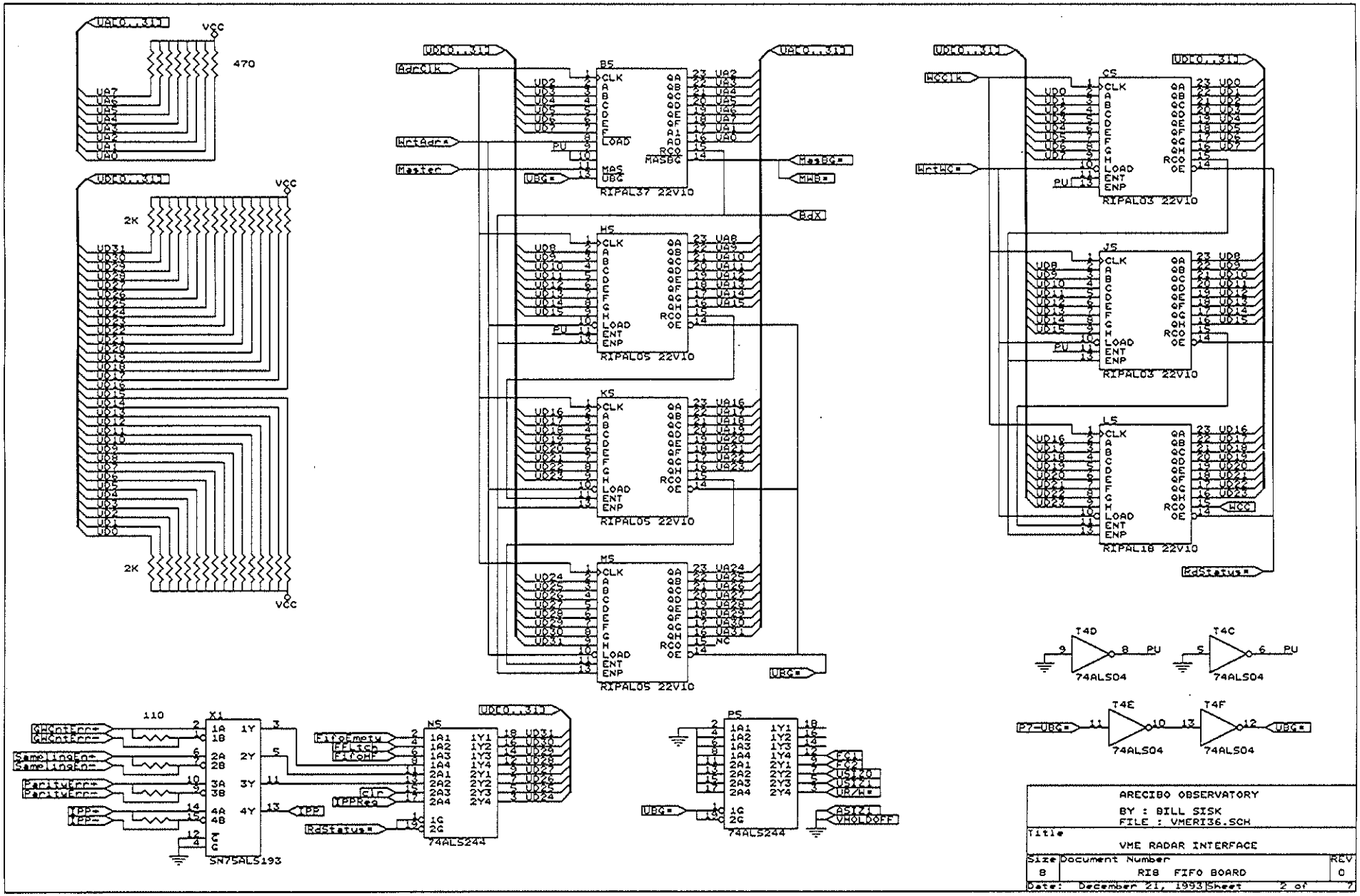

ARECIBO OBSERVATORY
BY : BILL SISK
FILE : VMERI35.SCH
Title
VME RADAR INTERFACE
Size B
Document Number
RI8 FIFO BOARD
Rev 10
Date: April 7, 1997
Sheet 1 of 7

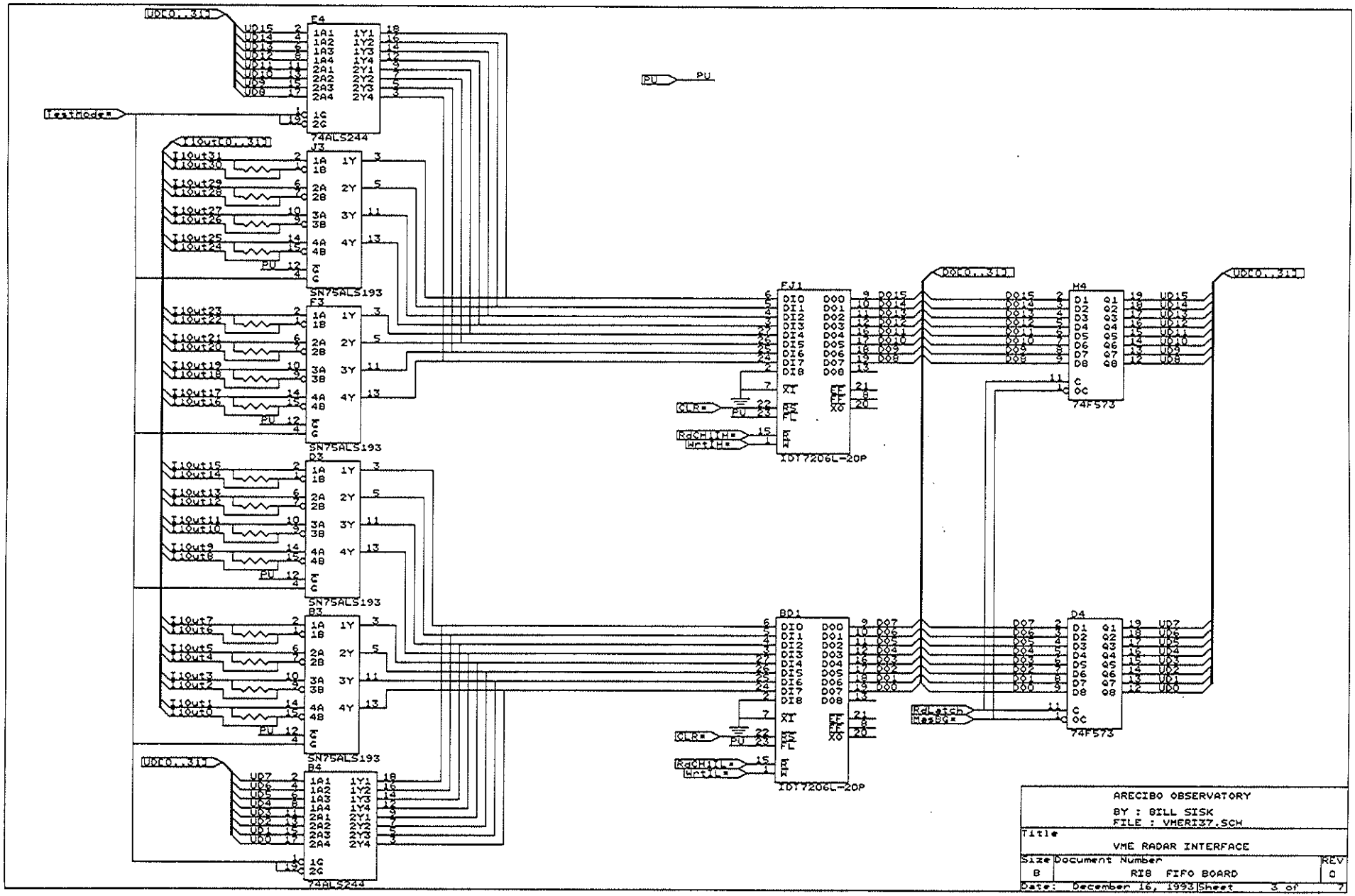

UDC0..31]
E4
74ALS244
TestMode*
I10out[0..31]
J3
SN75ALS193
F3
D3
B3
PU
FJ1
CY7C464-15PC
H4
74F573
BD1
D4
RdLatch
MasPC*
CLR*
RdCH1IH*
WrtIH*
RdCH1IL*
WrtIL*
B4
ARECIBO OBSERVATORY
BY : BILL SISK
FILE : VMERI37.SCH
Title
VME RADAR INTERFACE
Size
B
Document Number
RIB FIFO BOARD
REV
0
Date: May 13, 1994
Sheet 3 of 7

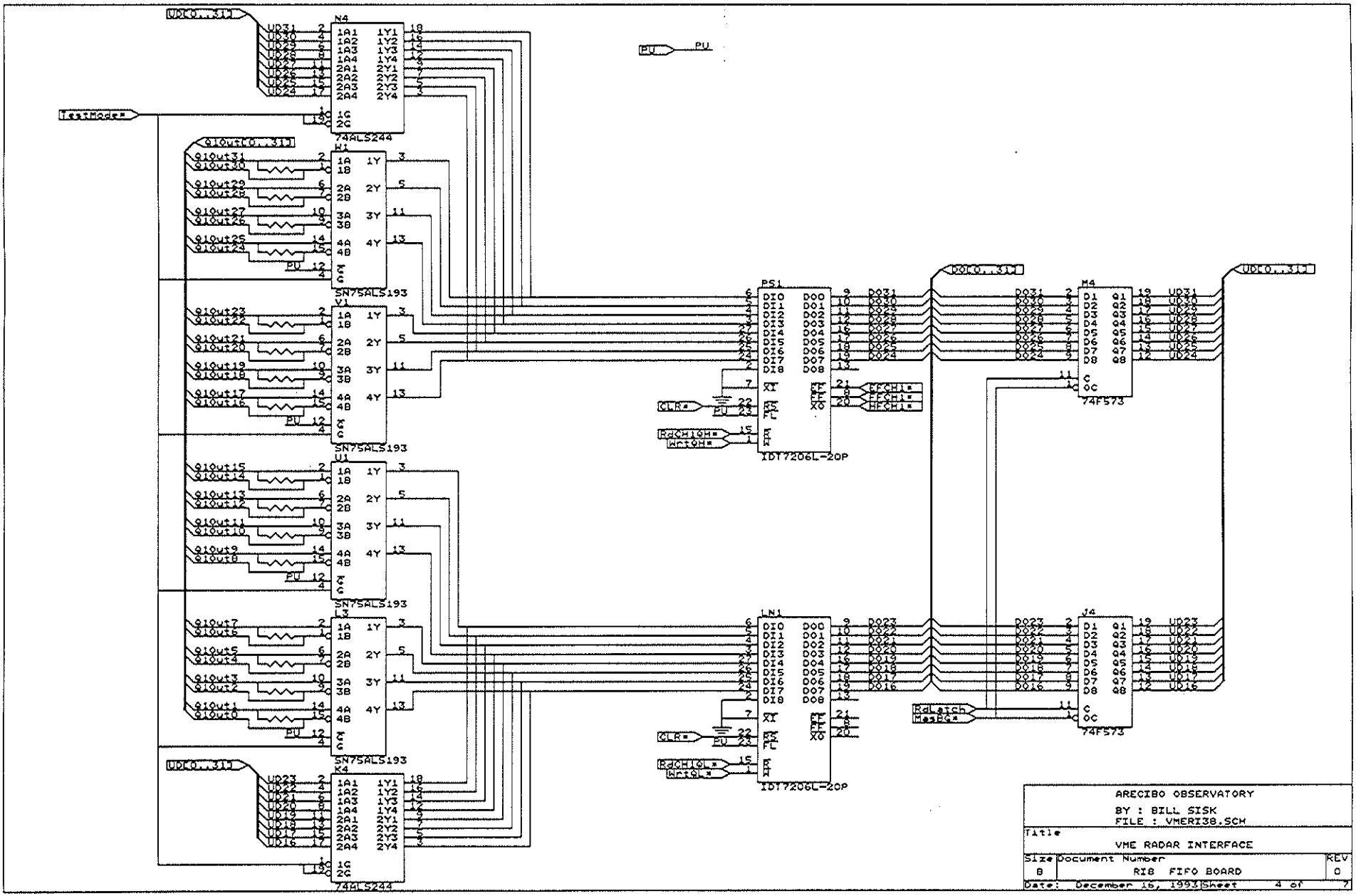

UD[0..31]
N4
74ALS244
TestMode*
PU
Q10out[0..31]
U1
V1
U4
L3
SN75ALS193
PS1
LN1
CY7C464-15PC
CLR*
RdCH10H*
WrtQH*
RdCH10L*
WrtQL*
EFCH1*
FFCH1*
HFCH1*
M4
J4
74F573
RdLatch
MasRG*
K4
ARECIBO OBSERVATORY
BY : BILL SISK
FILE : VMERI38.SCH
Title
VME RADAR INTERFACE
Size
B
Document Number
RI8 FIFO BOARD
REV
0
Date: May 13, 1994
Sheet 4 of 7

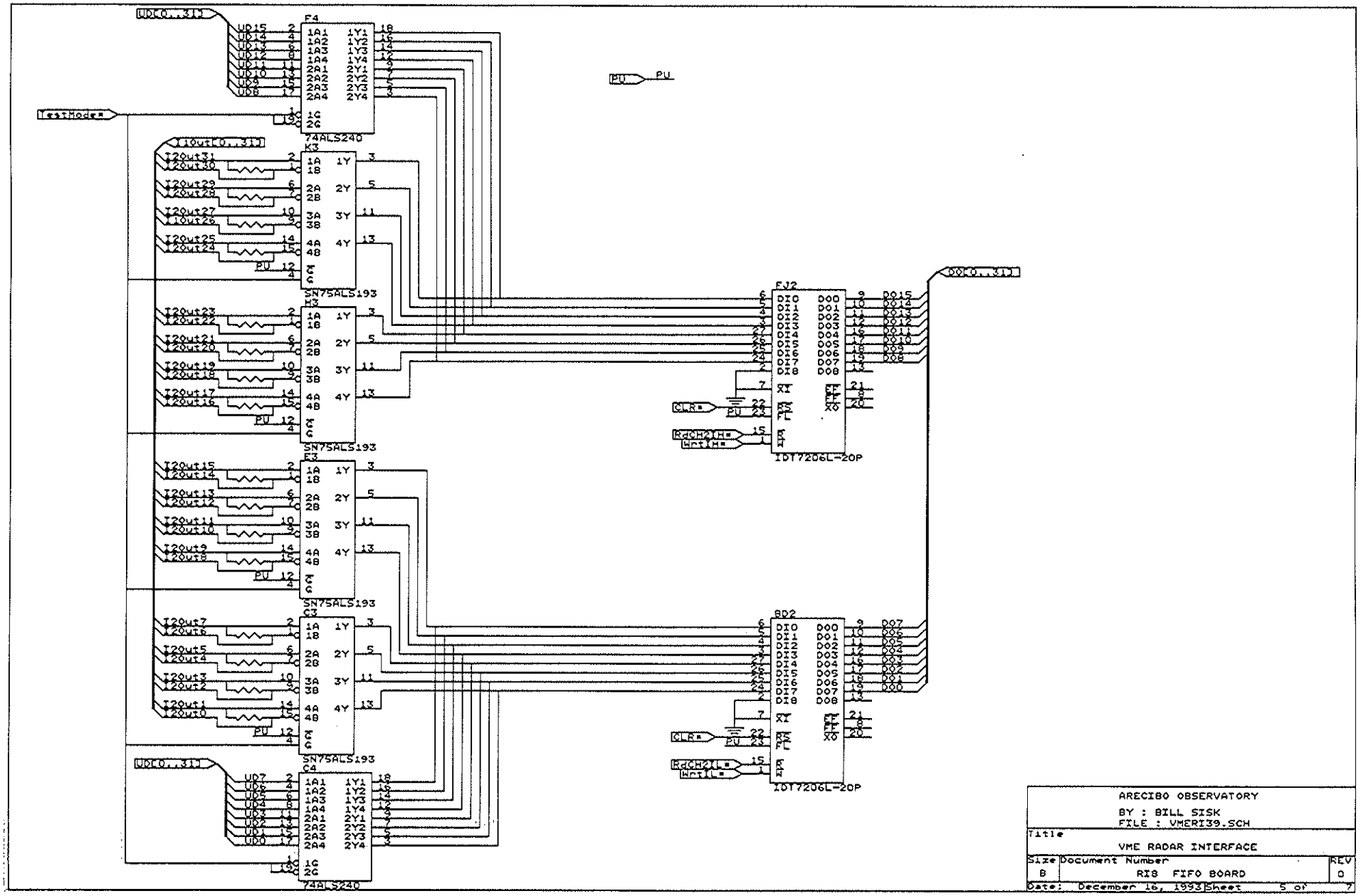

UD[0..31]
F4
74ALS240
TestMode*
I10ut[0..31]
K3
SN75ALS193
M3
SN75ALS193
P3
SN75ALS193
C3
SN75ALS193
PU
FJ2
CY7C464-15PC
DO[0..31]
CLR*
RdCH2H*
WrtH*
RD2
CY7C464-15PC
RdCH2L*
WrtL*
C4
74ALS240
AREC1B0 OBSERVATORY
BY : BILL SISK
FILE : VMERI39.SCH
Title
VME RADAR INTERFACE
Size B
Document Number
RI8 FIFO BOARD
REV 0
Date: May 13, 1994
Sheet 5 of 7


UD[0..31]
P4
74ALS240
TestMode*
PU
G10ut[0..31]
G20ut31
G20ut30
G20ut29
G20ut28
G20ut27
G20ut26
G20ut25
G20ut24
X2
SN75ALS193
G20ut23
G20ut22
G20ut21
G20ut20
G20ut19
G20ut18
G20ut17
G20ut16
W2
SN75ALS193
G20ut15
G20ut14
G20ut13
G20ut12
G20ut11
G20ut10
G20ut9
G20ut8
V2
SN75ALS193
G20ut7
G20ut6
G20ut5
G20ut4
G20ut3
G20ut2
G20ut1
G20ut0
U2
SN75ALS193
L4
74ALS240
PS2
CY7C464-15PC
LN2
CY7C464-15PC
DO[0..31]
CLR*
RdCH2OH*
WrtOH*
RdCH2OL*
WrtOL*
FFCH2*
FFCH2
HFCH2*
AREC1B0 OBSERVATORY
BY : BILL SISK
FILE : VMERI40.SCH
Title
VME RADAR INTERFACE
Size
B
Document Number
RIB FIFO BOARD
REV
0
Date:
May 13, 1994
Sheet
6 of 7

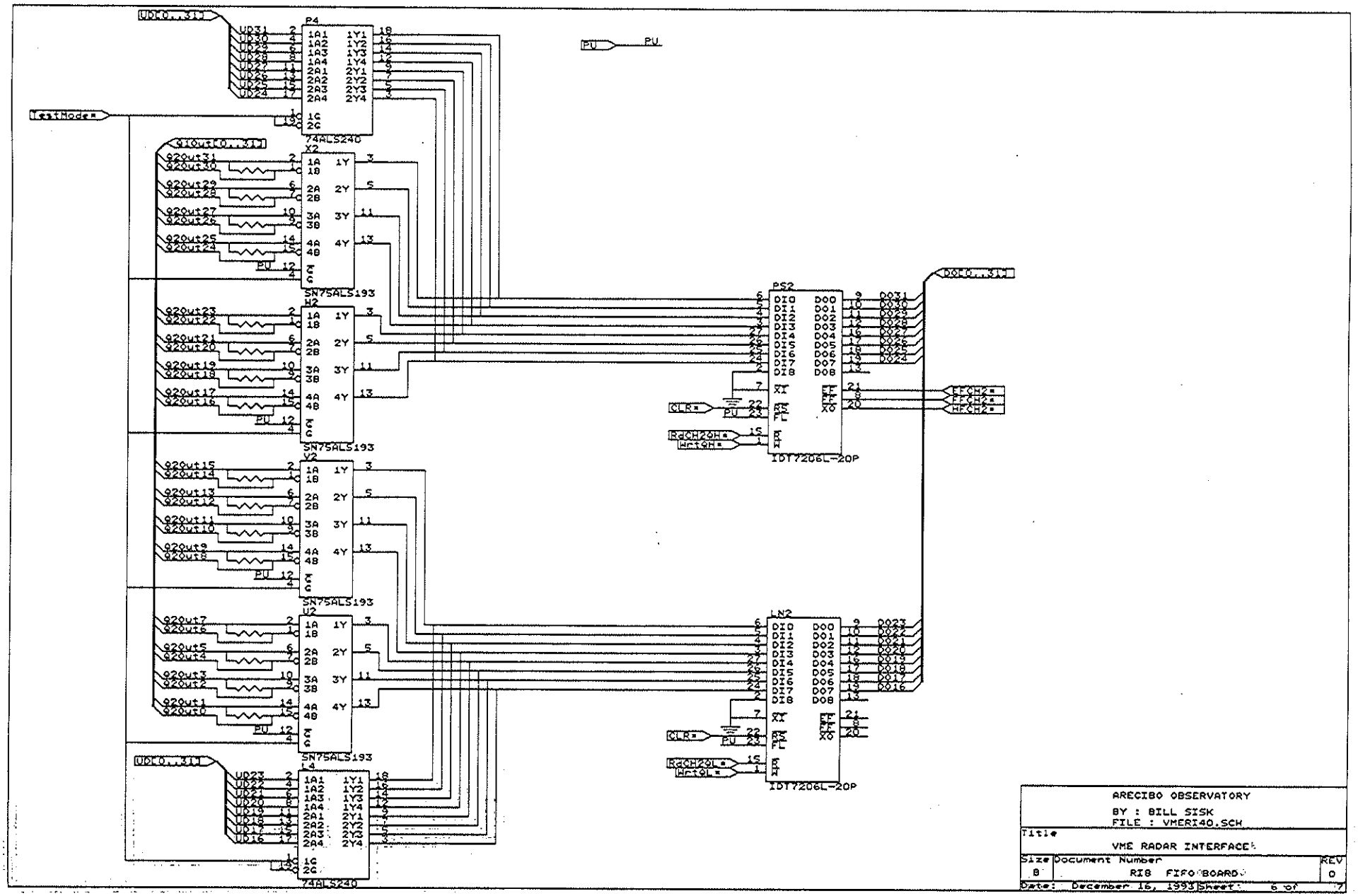

ARECIBO OBSERVATORY
BY : BILL SISK
FILE : VMERI36.SCH
Title
VME RADAR INTERFACE
Size B
Document Number RI8 FIFO BOARD
REV 0
Date: December 21, 1993 Sheet 2 of 7
RIPAL37 22V10
RIPAL05 22V10
RIPAL03 22V10
RIPAL18 22V10
74ALS04
74ALS244
SN75ALS193

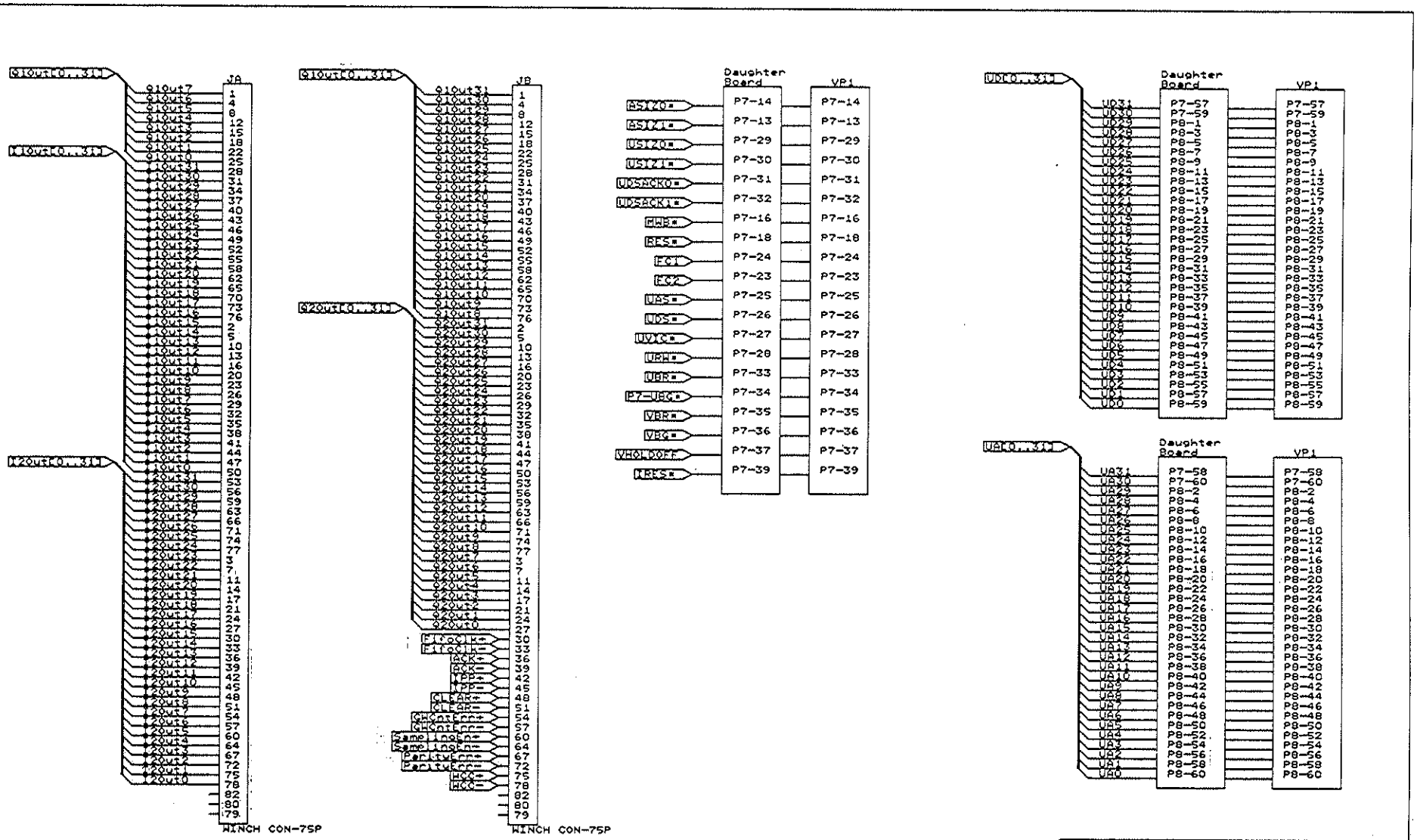

ARECIBO OBSERVATORY
BY : BILL SISK
FILE : VMERI37.SCH
Title
VME RADAR INTERFACE
Size B
Document Number RI8 FIFO BOARD
REV 0
Date: December 16, 1993 Sheet 3 of 7
74ALS244
SN75ALS193
IDT7206L-20P
74F573
TestMode*
PU
RdCH1H*
WrtH*
RdCH1L*
WrtL*
RdLatch
MasBy*
CLR*


UD[0..31]
N4
74ALS244
TestMode*
Q10out[0..31]
H1
SN75ALS193
V1
U1
L3
K4
PU
P5i
IDT7206L-20P
CLR*
RdCH1QH*
WrtQH*
RdCH1QL*
WrtQL*
D[0..31]
M4
74F573
L4i
J4
RdLatch*
WrtPC*
ARECIBO OBSERVATORY
BY : BILL SISK
FILE : VMERI38.SCH
Title
VME RADAR INTERFACE
Size B
Document Number RI8 FIFO BOARD
REV 0
Date: December 16, 1993 Sheet 4 of 7



ARECIBO OBSERVATORY		
BY : BILL SISK		
FILE : VMERI39.SCH		
Title: VME RADAR INTERFACE		
Size: B	Document Number: RIS FIFO BOARD	REV: 0
Date: December 16, 1993	Sheet 5 of 7	


UD[0..31]
P4
74ALS240
TestMode*
PU
D0[0..31]
920ut[0..31]
X2
SN75ALS193
M2
SN75ALS193
V2
SN75ALS193
U2
SN75ALS193
L4
74ALS240
PS2
IDT7206L-20P
LN2
IDT7206L-20P
CLR*
RdCH2SH*
WrtSH*
RdCH2SL*
WrtSL*
EFCH2*
FFCH2*
HFCH2*
ARECIBO OBSERVATORY
BY : BILL SISK
FILE : VMERI40.SCH
Title
VME RADAR INTERFACE
Size
B
Document Number
RI8 FIFO BOARD
REV
0
Date: December 16, 1993
Sheet 6 of 7


Q10out[0..31]
Q10out7
JA
WINCH CON-75P
Q10out[0..31]
Q20out[0..31]
JB
WINCH CON-75P
Daughter Board
VP1
ASIZ0*
ASIZ1*
USIZ0*
USIZ1*
UDSACK0*
UDSACK1*
RWB*
RES*
FC1
FC2
UAS*
UDS*
UVIC*
UBR*
UBG*
UBR*
P7-USG*
VBR*
VBG*
VHOLDOFF
IRES*
P7-14
P7-13
P7-29
P7-30
P7-31
P7-32
P7-16
P7-18
P7-24
P7-23
P7-25
P7-26
P7-27
P7-28
P7-33
P7-34
P7-35
P7-36
P7-37
P7-39
UDI0..31
UAI0..31
P8-1
P8-2
P8-3
P8-4
P8-5
P8-6
P8-7
P8-8
P8-9
P8-10
P8-11
P8-12
P8-13
P8-14
P8-15
P8-16
P8-17
P8-18
P8-19
P8-20
P8-21
P8-22
P8-23
P8-24
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RIB FIFO BOARD - CONNECTOR DIAGRAM
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Date: December 16, 1993 Sheet 7 of 7