Digital Signal Processing Using CASPER Tools (AO-6)

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Project Description

Introduction to **CASPER** hardware a software tools, particular focus in **ROACH 1**, **iADC** and **katADC**. We are going to be using the **MSSGE** toolflow to generate **configuration files** for the **FPGA**, and **Python** scripts for configuration and data capture.

The intention is to **digitize a simulated bandpass**, do some **digital signal processing** and **send and capture the data** in a computer.

During hands-on data-reduction times

CASPER Group

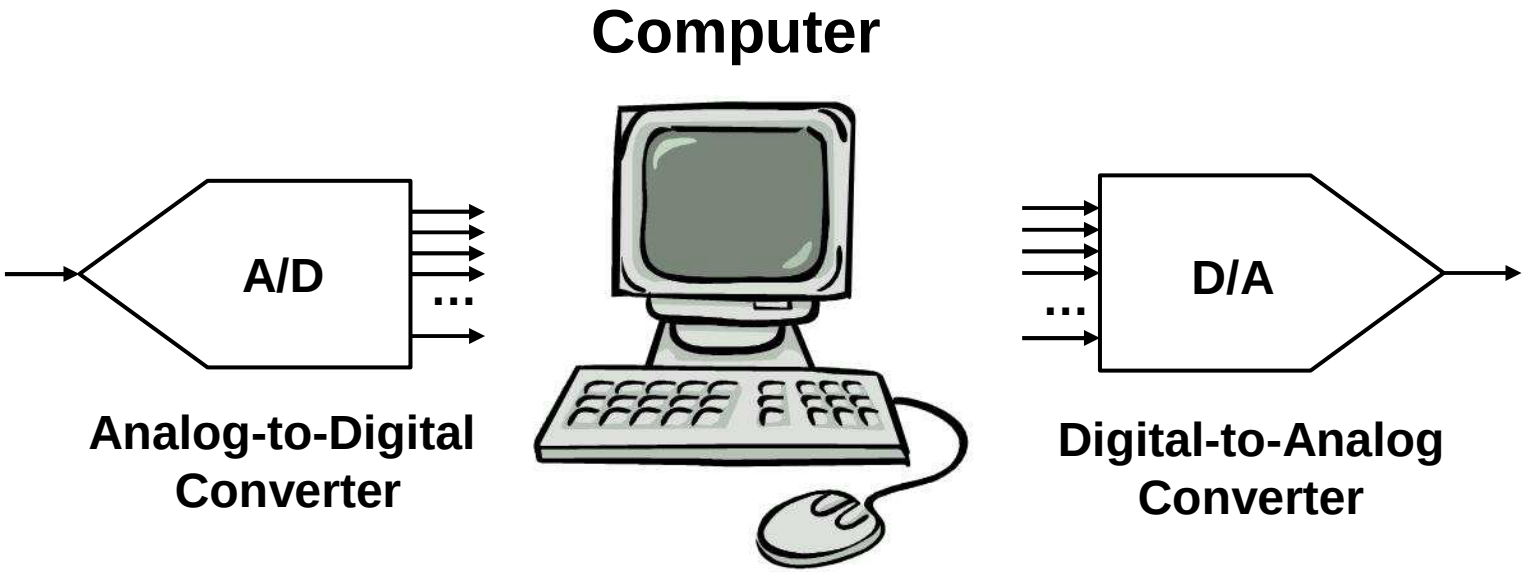
CASPER
COLLABORATION FOR ASTRONOMY SIGNAL PROCESSING AND ELECTRONICS RESEARCH

Open source hardware and software tools for Digital Signal Processing (DSP) instrumentation:

Web site: https://casper.berkeley.edu/

Mailing list:casper@lists.berkeley.edu

Digital Signal Processing System



Data Storage
Data Processing
- **Math Operations**
- **Filters**
- **Fourier Transform**
- **Data Format**

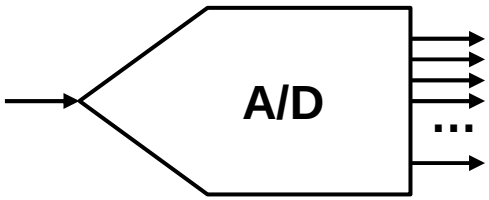
Computer
- **Micro Processor**
- **DSP (MAC)**
- **FPGA**

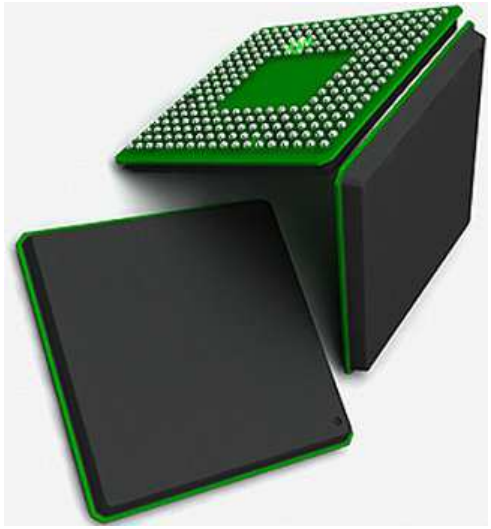
Digital Signal Processing System using FPGA

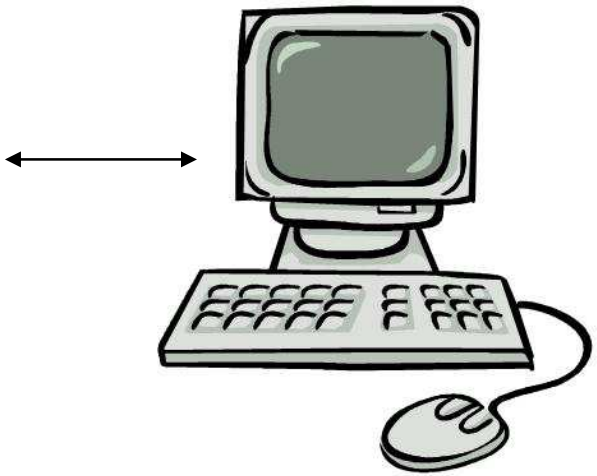
Analog-to-Digital Converter

Field-Programmable Gate Array

Computer







CASPER

USER

- Interface
- Data Format
- Communication
- DSP Algorithms

- Development
- Configuration
- Data Storage

CASPER Hardware

Web site: https://casper.berkeley.edu/

Go to: Documentation >> Hardware

Processing Boards

- IBOB (2005 - present | Virtex-II Pro)
- BEE2 (2005 - present | 5x Virtex-II Pro)
- ROACH (2009 - present | Virtex 5 SXT95/LXT110/LXT155)
- ROACH2 (2010 | Virtex 6)
- ROACH-2 Revision 2 (2012 | Virtex 6)

Mezzanine Boards

- CX4 (3 x CX4 Mezzanine board)
- SFP+ (Quad SFP+ Mezzanine board)

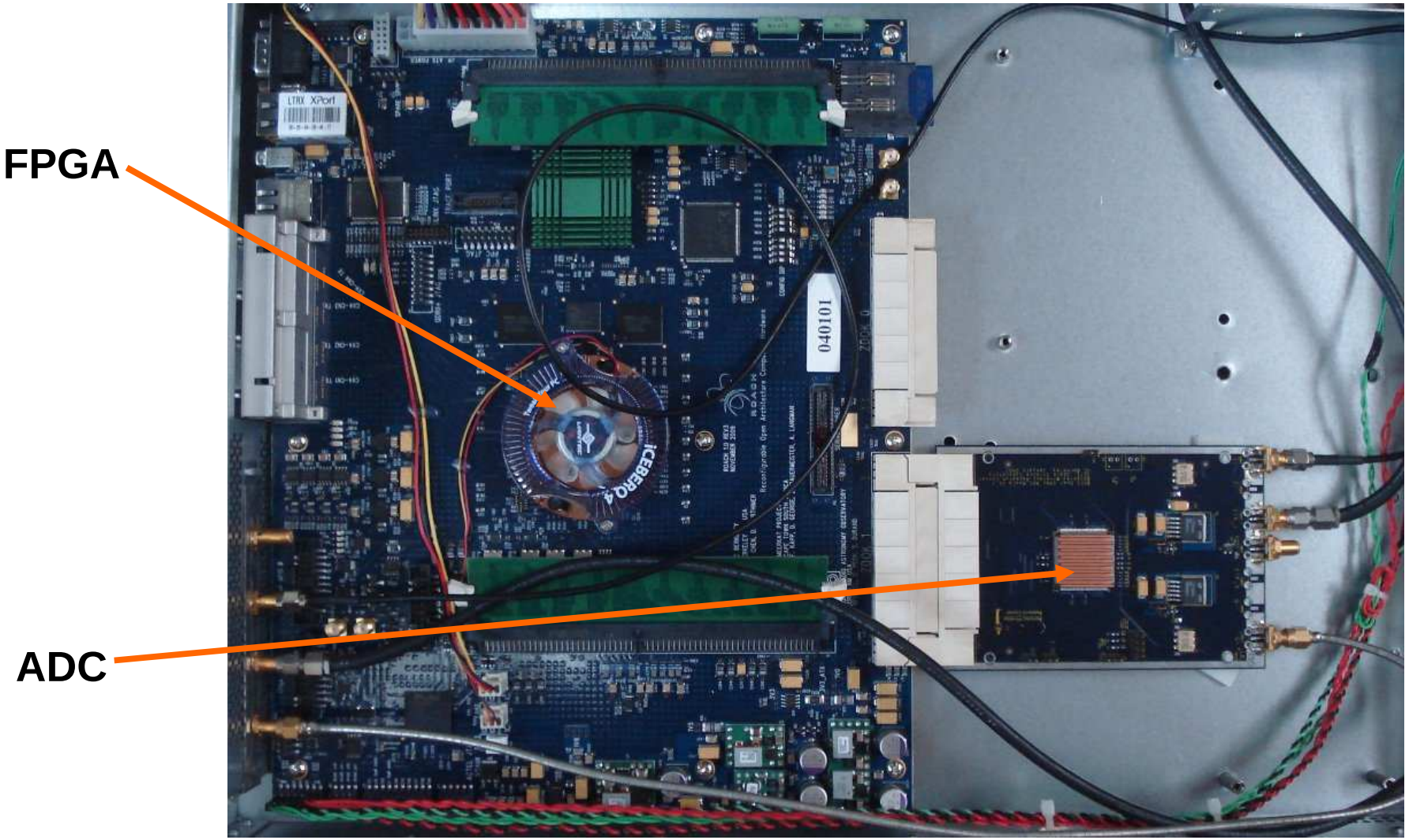
ADC Boards

- ADC2x1000-8 (2005 - present | dual 1GSa/sec)
  Dual 8-bit, 1000Msps (or single 8-bit 2000Msps)
- ADC1x3000-8 (2007 - present | 3GSa/sec)
  Single-8 bit, 3000Msps National ADC083000 ADC
- 64ADCx64-12 (2008 - present | 64x 50MSa/sec)
  64 inputs, 64 Msps, 12 bit, double wide board
- ADC4x250-8 (2008 - present | quad 250MSa/sec)
  Quad 8-bit, 250 Msps, Analog Devices AD9480 ADC
- ADC2x550-12 (2009 - present | dual 550 Msps)
  Dual 12-bit, 550 Msps, TI ADS54RF63I
- ADC2x400-14 (2009 - present | dual 400 Msps)
  Dual 14-bit, 400 Msps, TI ADS5474
- KatADC (2010 - present | dual 1.5GSPS or single 3.0GSPS)
  Dual 8-bit 1.5GSPS (or Single 8-bit 3.0GSPS)
- ADC1x5000-8 (2010-present | Single 5.0 or dual 2.5 GS/s, 4/8 bit
- Next Generation Samplers (2011+ | >3GSPS)
- ADC16x250-8 (Q2 2012 - present)
  16,8,4 inputs 8 bits 250,500,1000 MSPS, Hittite HMCAD1511
- ADC1x10000-4 (2012-present | Single 10.0 GS/s, 4 bit versions)
- ADC1X2200-10 (2012 - present | Single 2.2GSPS, 10-bit)
  Single 10-bit 2.2GSPS, e2v AT84AS008 ADC & AT84CS001
- DAB-HERALD (2013 - | 8 x 250 Msps, 4 x 500 Msps
  RF-to-packet converter using 2 x HMCAD1511

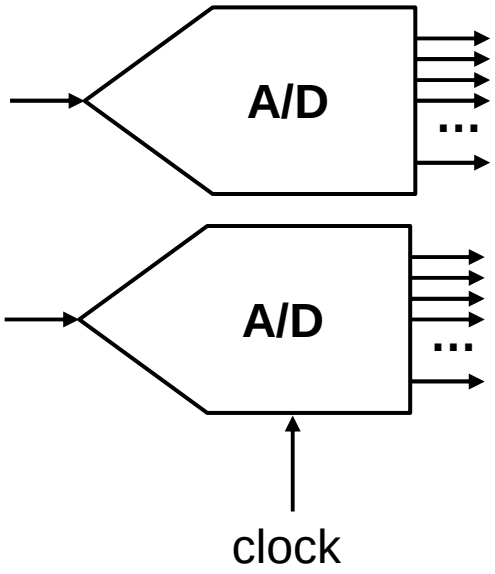
DAC Boards

- DAC2x1000-16
  Dual 16-bit, 1000 Msps, TI DAC5681

CASPER Hardware – ROACH + iADC



Analog to Digital Converter - ADC



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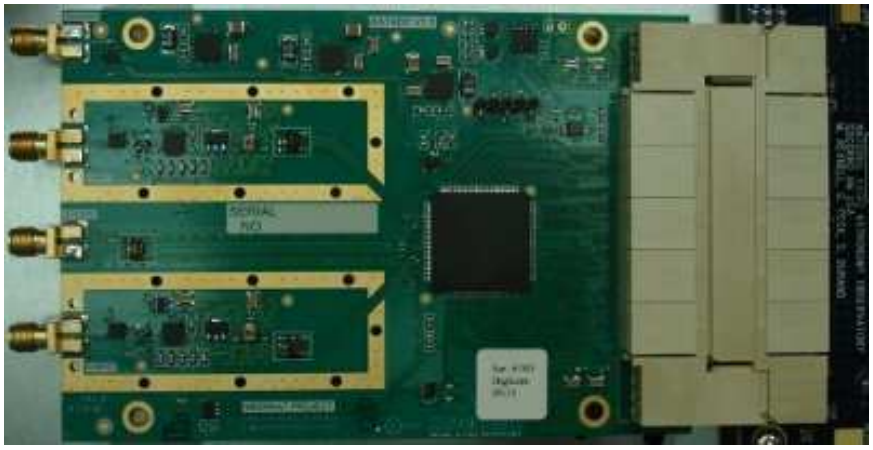
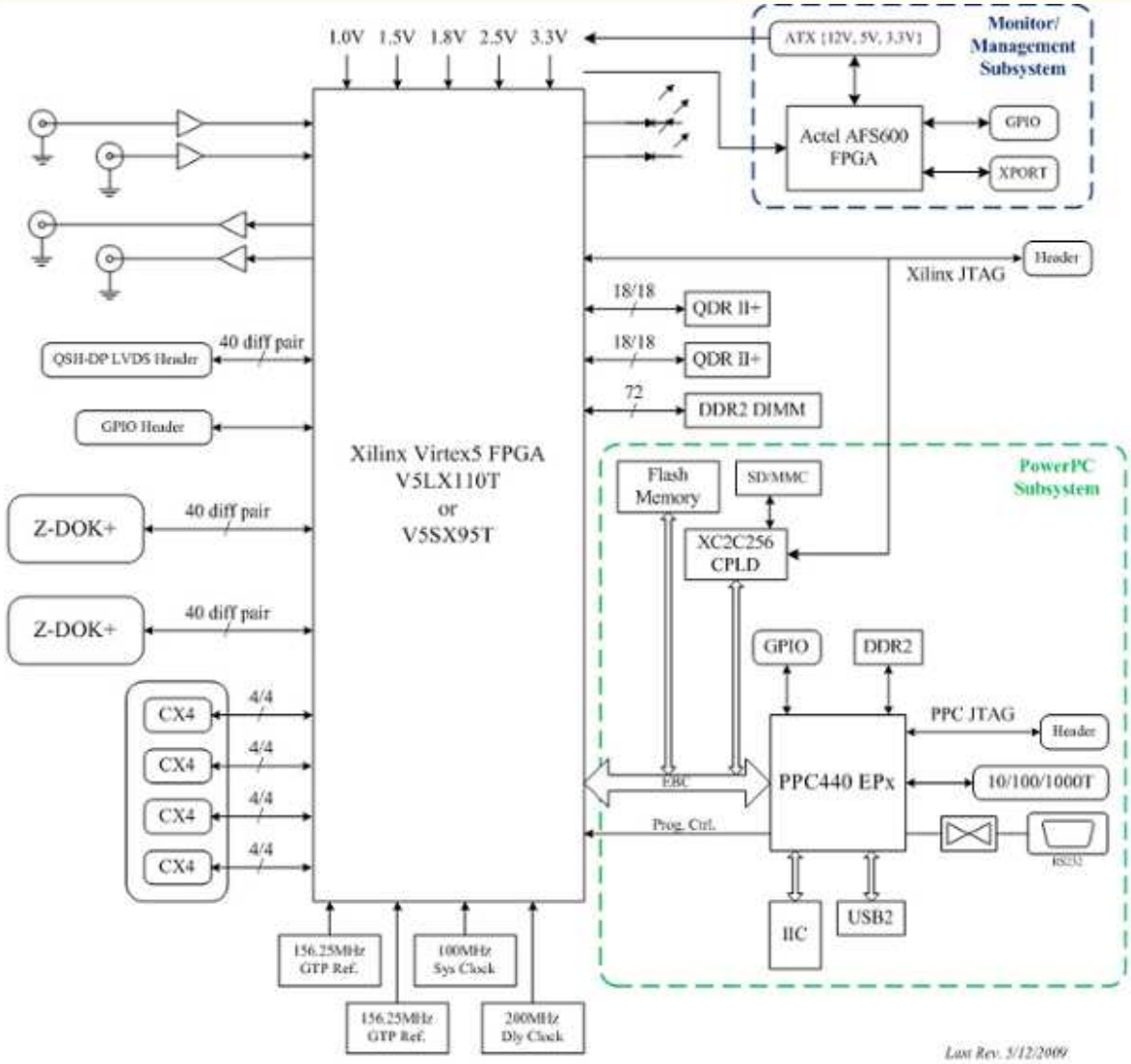
iADC (ADC2x1000-8)

or

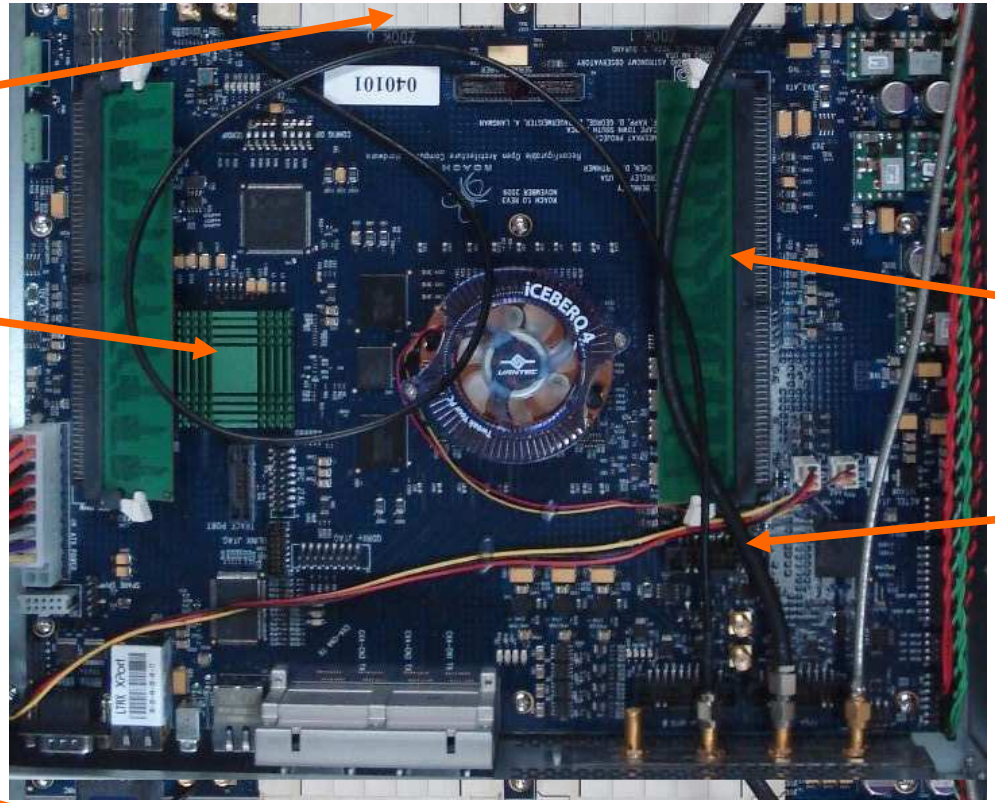
katADC



ROACH (Reconfigurable Open Architecture Computing Hardware)



ROACH (Reconfigurable Open Architecture Computing Hardware)



Z-DOK+

PowerPC

Mem

DIO

CX4

Ethernet

RS232

ADC

CASPER Software

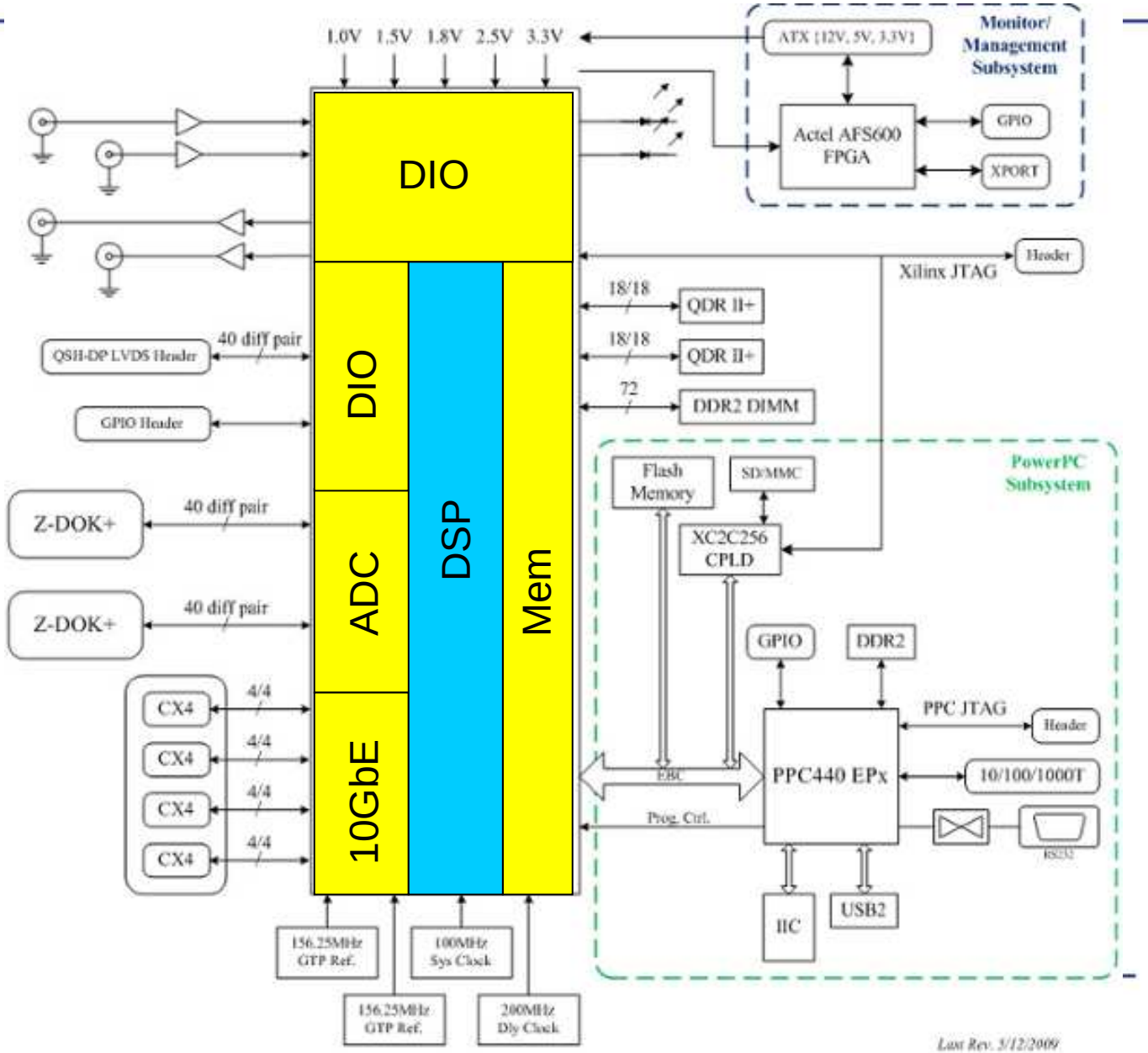
MSSGE Toolflow

- **M**atlab
- **S**imulink
- **S**ystem **G**enerator

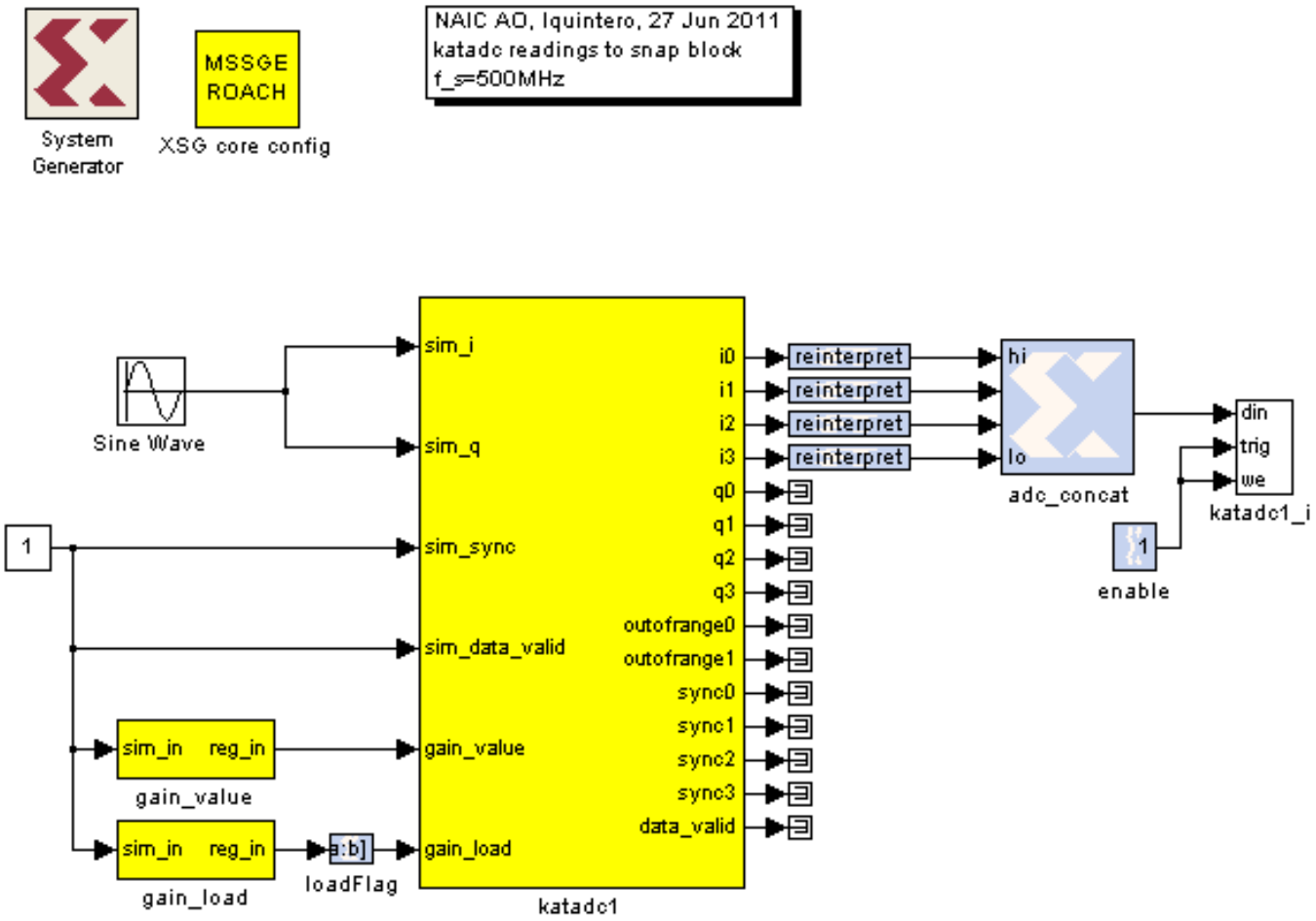
- **E**DK

CASPER Libraries

CASPER Libraries



MSSGE and Libs in Action – Raw Data Capture



CASPER Software Installation

11.x - Stable/Production (RHEL5 / CentOS)*

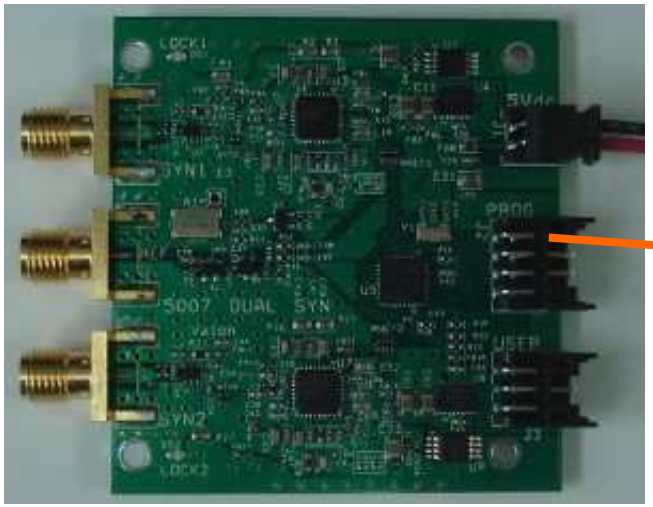
Required software**

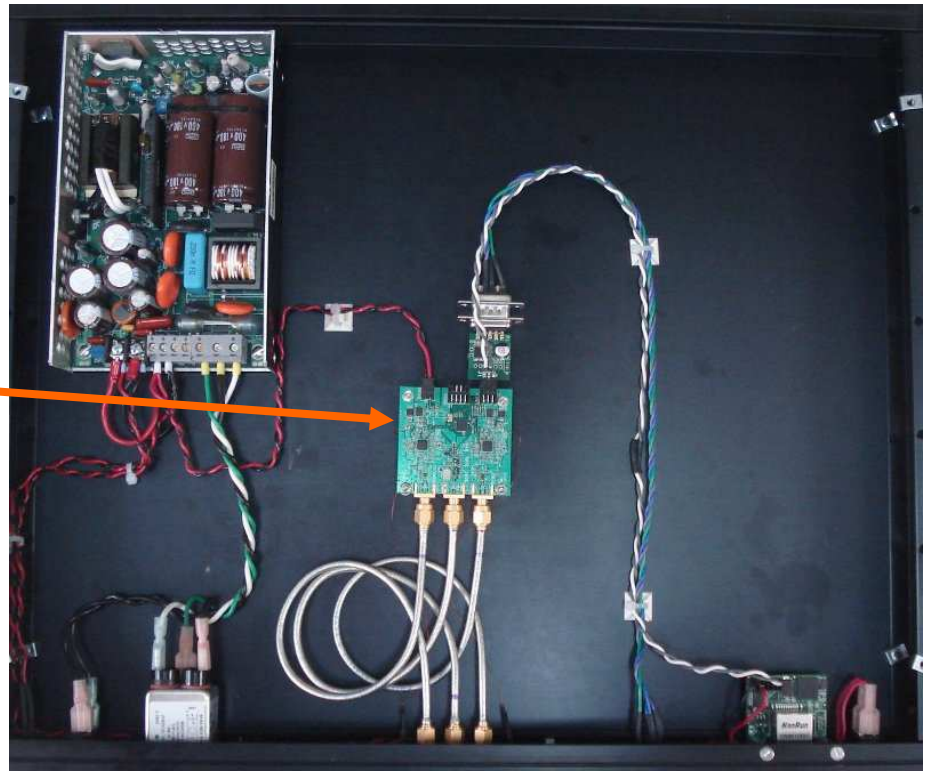
- Matlab R2008a or R2008b (v7.7.0)
- Simulink R2008b (v7.2)
- Xilinx System Generator v10.1.3.1386
- Xilinx EDK v11.5
- Xilinx ISE v11.5
- MSSGE libraries

* https://casper.berkeley.edu/wiki/Xilinx_ISE_11.4_Setup

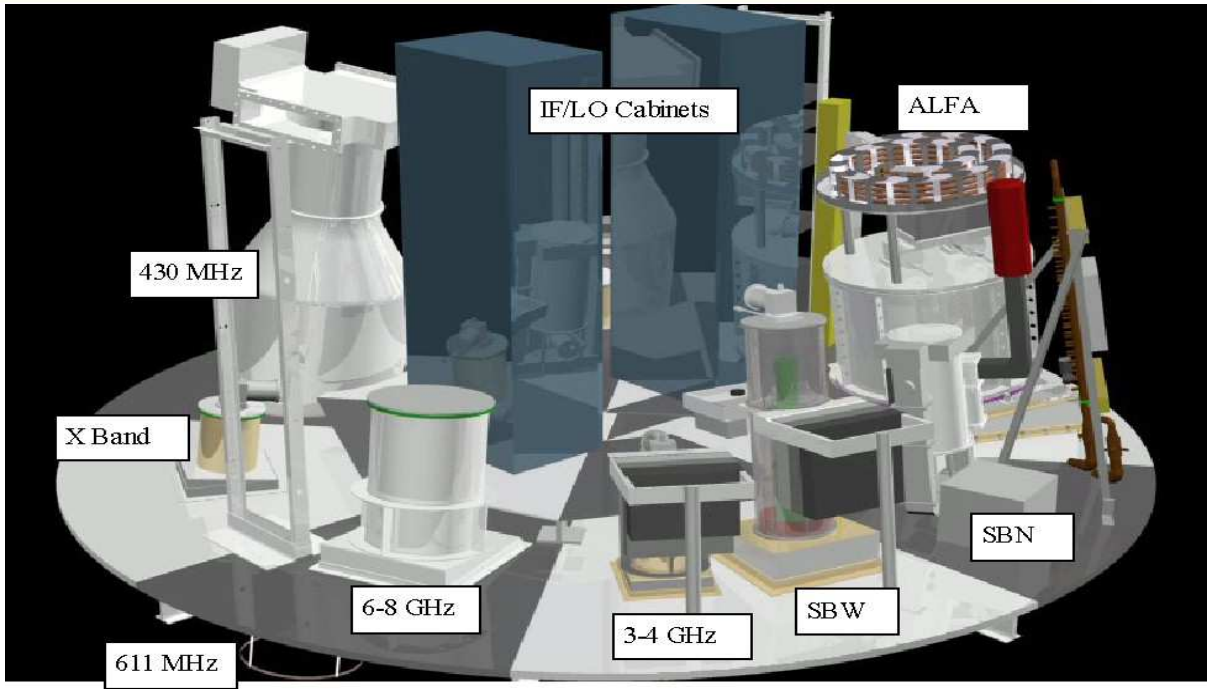
** https://casper.berkeley.edu/wiki/MSSGE_Toolflow_Setup

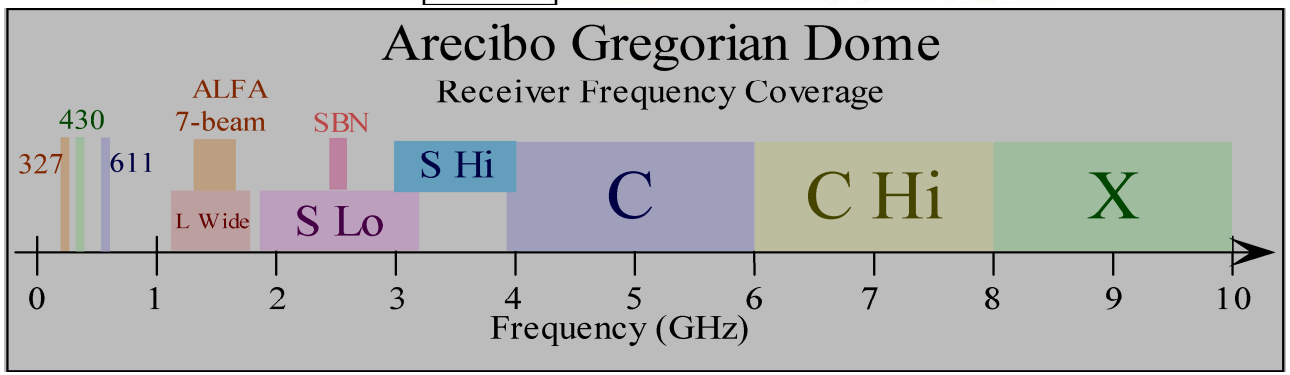
Clocking – Valon 5007





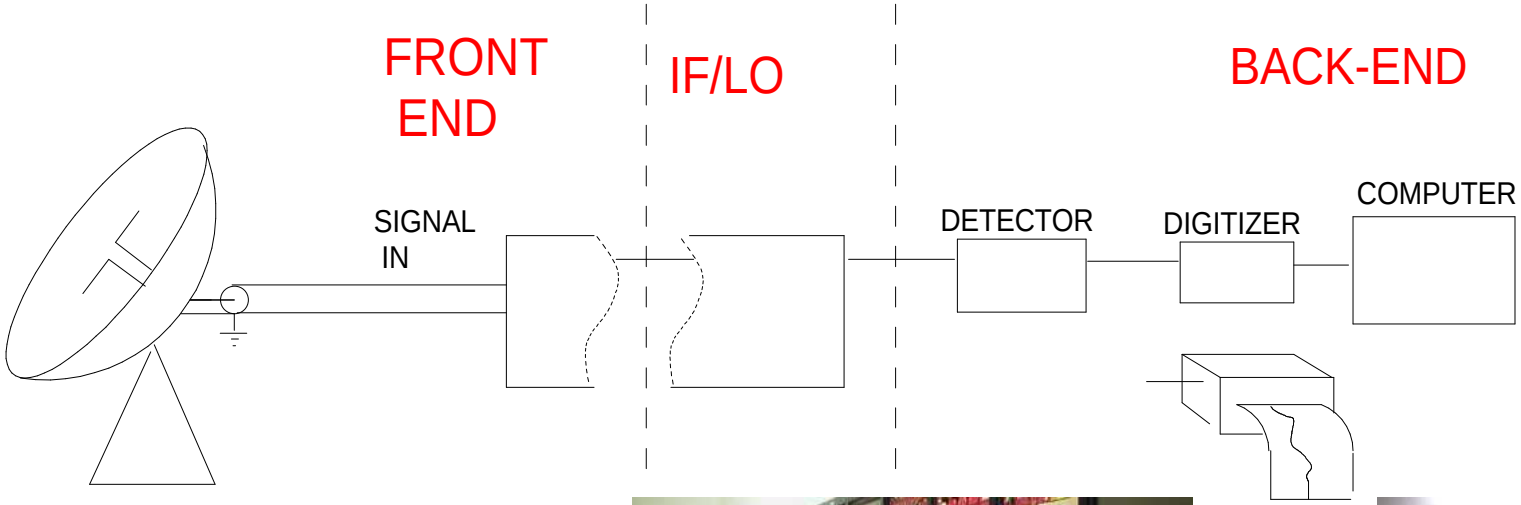
Gregorian Dome Receivers

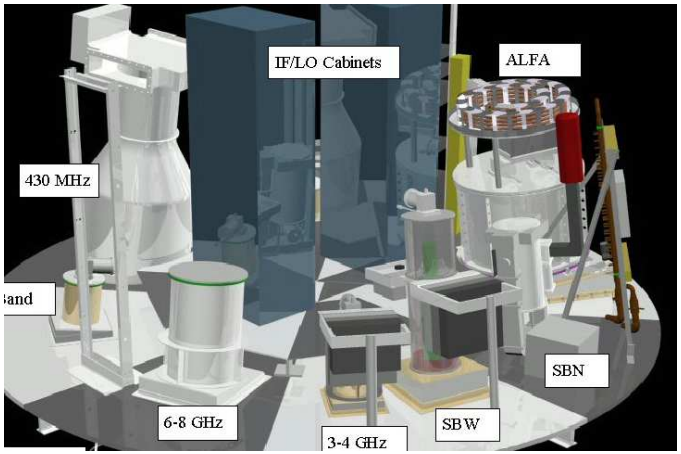




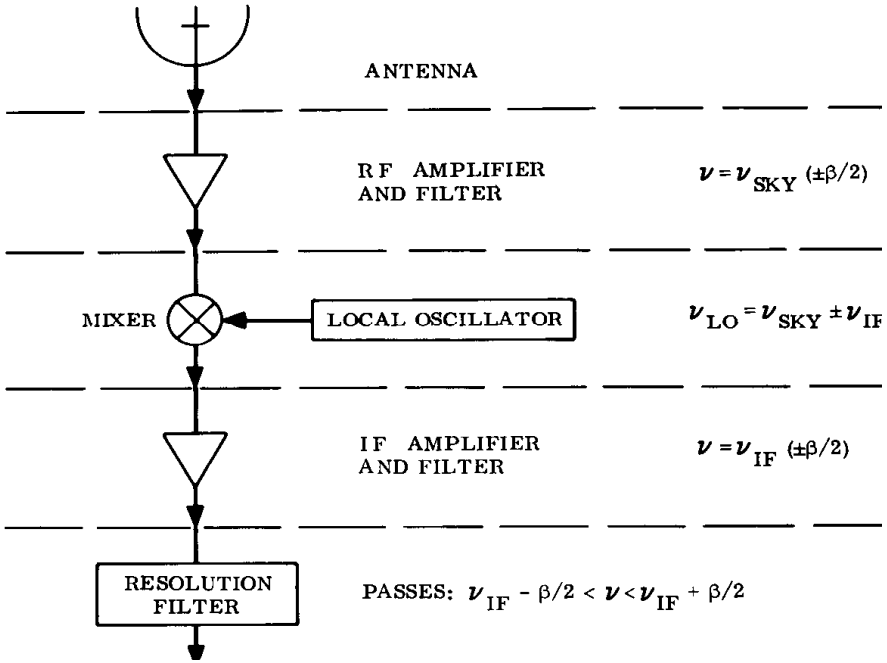
Ganesan, R. "Telescope Electronics", May 2006

Radio Frequency Signal Path

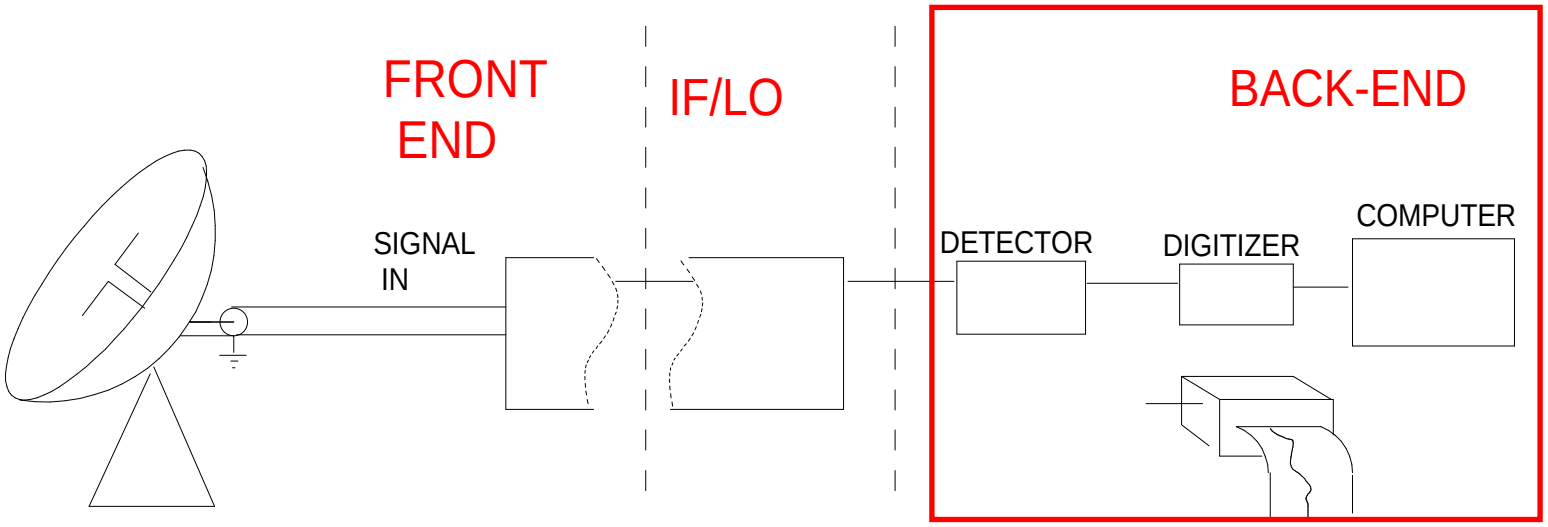




Signal Transport – Intermediate Freq.

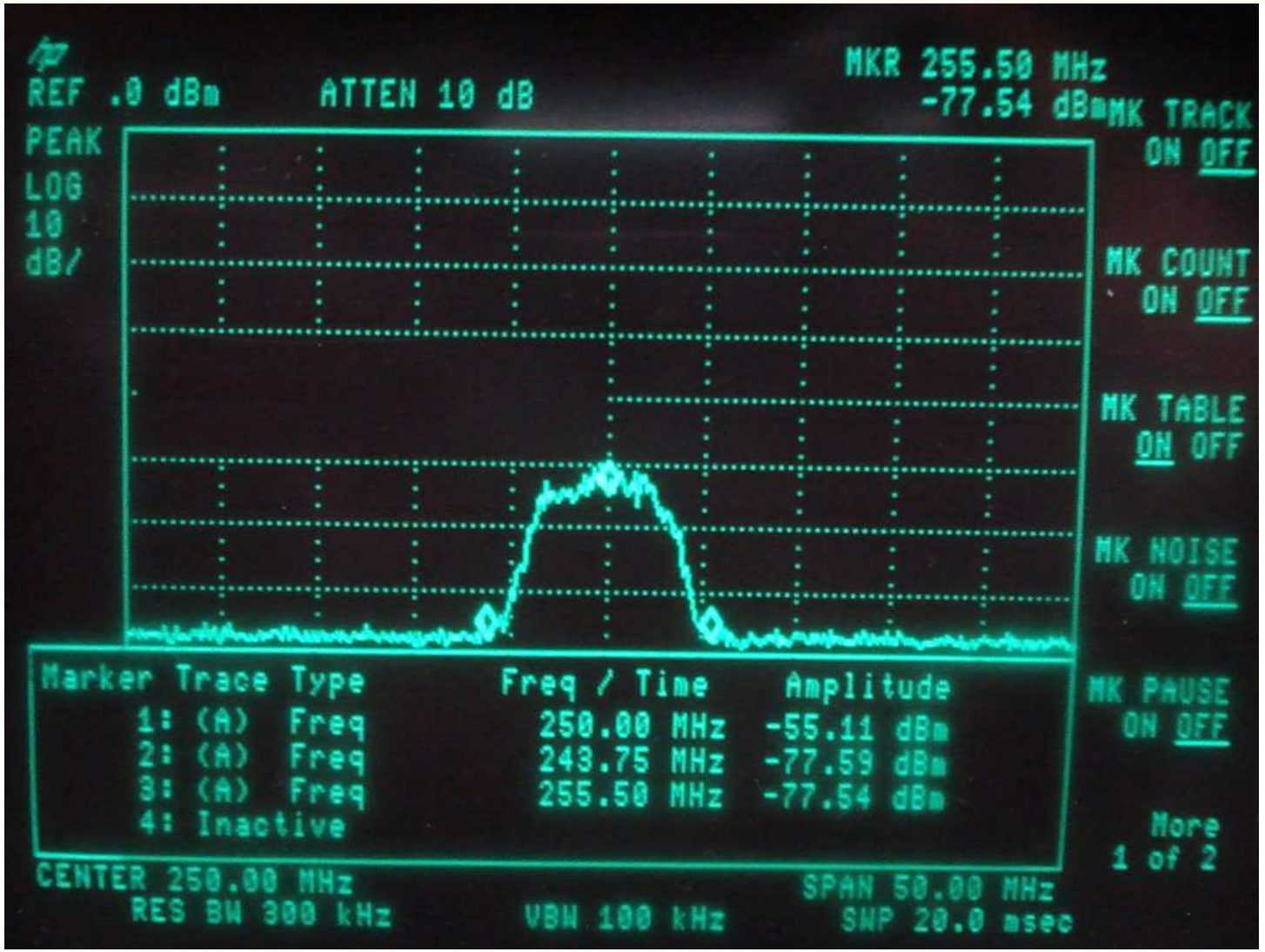


Final Stage – Data Acquisition



Data Sampling and Storage

Test Signal – Bandpass



SDSS7 Schedule – Hands-on Project

- Thu, 11 Jul.
  - 1630 – 1730. Logistics
  - 1730 – 1900. Planning.
- Sun, 14 Jul.
  - 1330 – 1500. Hardware and Software tools.
  - 1530 – 1730. FPGA Synthesis and Configuration.
- Mon, 15 Jul.
  - 1300 – 1500. Python Utils and Raw Data Capture.
  - 1630 – 1730. DSP Design
- Tue, 16 Jul.
  - 0830 – 1000. DSP Design
  - 1030 – 1200. Presentation Preparation (PP).
  - 1330 – 1400. PP and Load Talks.
  - 1400 – 1530. Presentations (5min talks)

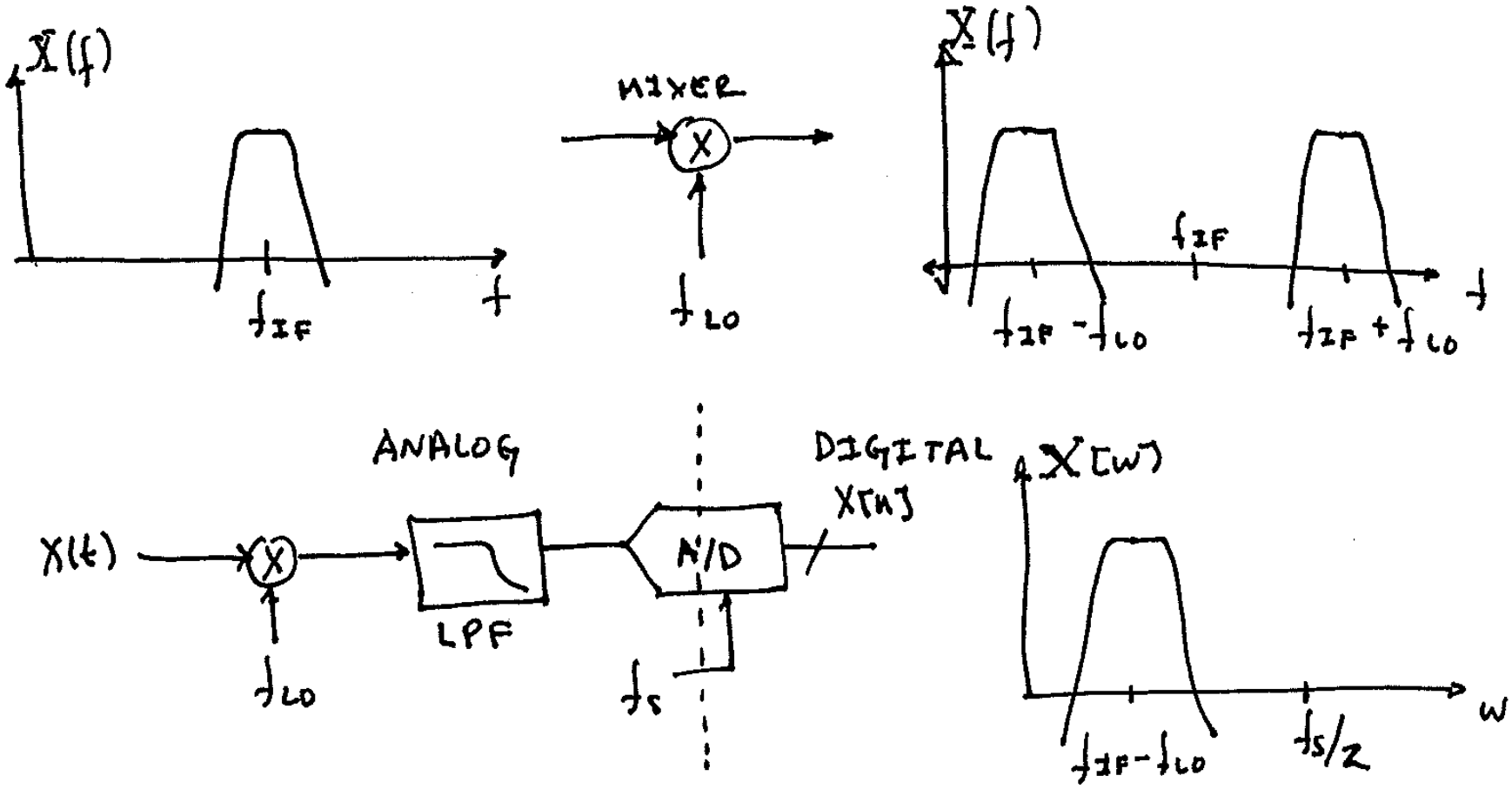
Participants Interest and Background

- What is your interest of doing this hands-on project?
- What programming language(s) are familiar for you?
- Do you have experience in electronics or DSP systems?
- Are you familiarized with CASPER tools?
  - What projects?
  - Any special interest during this week?

Potential Projects

- Digital Down Conversion
- CASPER Tutorials – FFT

Down Conversion



Digital Down Conversion