

Arecibo Upgrade Notes
A DFT FILTER BANK BASED ON THE AUSTEK CHIP:
II. HARDWARE IMPLEMENTATION

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INTRODUCTION

The 430 MHz system at Arecibo will continue to be the most sensitive system even after the upgrade and it is expected to be heavily used for pulsar work. Here we outline a plan for building an FFT-based system that is aimed primarily at pulsar searching over the 10 MHz feed bandwidth, but will also be useful for timing and polarization studies. For pulsar searching, the device can provide 1024 spectral channels (10 kHz each) every $100\mu\text{s}$, matched to dispersion measures up to 100 pc cm^{-3} . Timing and polarization studies may be performed with better time resolution by decreasing the FFT length, allowable on pulsars with $\text{DM} < 100\text{ pc cm}^{-3}$. This project is intended to complement other hardware developments in the pulsar community and at NAIC, including the Berkeley CDRP project, the Caltech FPTM, and a search/timing machine based on the new NAIC/NASA 50 MHz correlator chip.

While motivated by 430 MHz pulsar science, the proposed system can certainly be used at other frequencies and can be used to cover 20 MHz total bandwidth in two polarizations of undersampling of the FFTs is allowable. As configured, the proposed system will also be of general use wherever a power spectrum (or the complex FFT) is desired.

For pulsar science, in a related document, **A DFT FILTER BANK BASED ON THE AUSTEK CHIP: I. BASIC CONSIDERATIONS**, I outline achievable time resolutions, including a discussion of interstellar scattering, the need for overlapped transforms, and data rates. Here, we discuss hardware implementation of the device.

THE AUSTEK A41102 CHIP

The FFT chip performs 2 to 256 point DFT's on up to 24-bit input data (in each of I and Q) over bandwidths as large as 2.5 MHz, yielding complex output with ≤ 24 bit precision. The implementation we propose consists of 8-bit input data and 16-bit data out of the chip. The net precision out of an accumulator/packer board will most likely be much smaller, two bits, say. I/O is configured so that a window may be applied to the input or the output data. With full-length FFTs, a complete FFT is produced every $102.4\mu\text{s}$.

FFT BOARDS

A basic one-chip board is being designed by Paul Horowitz and Jon Weintroub at Harvard. The board allows a broad range of spectroscopic and pulsar observations. The board can operate with a default set of parameters uploaded to the FFT chip from ROM, including a time-domain window. All chip parameters can be controlled externally via serial port commands to a microcontroller. Input to the board consists of 16 bit complex samples (I and Q) with one parity bit. Output from the chip may be processed on-board in two ways: (1) squared-magnitude computation ($I^2 + Q^2$) combined with accumulation of a number of individual spectra (up to ~ 128 sec) in a multiply-accumulator (MAC); or (2) output of complex samples without accumulation. Partial board tests may be invoked through appropriate commands that test the FFT, squaring, and accumulation. End-to-end tests can be made through test signals injected at IF or baseband externally to the spectrometer. Synchronization of I/O and accumulation takes into account the choice of FFT length. Data acquisition is synchronized to external signals (eg. a 10-sec tick) by a 'vector-warning' signal that designates the beginning of a data vector to be transformed. Once initiated, the chip will free-run until commanded to do otherwise. Time tagging, data packing, and resampling is done on an auxiliary board, the accumulator/packer board. However, pairs of boards may be run on the same input data signal to yield FFT's from data spans that overlap by 50 data that more nearly satisfy the sampling theorem.

A control bit determines if a board waits for half an accumulation before initiating the computation of an FFT.

A 10 MHz BANDWIDTH PULSAR MACHINE

FFT boards are fed by digitized signals from an external device. The current plan is to use downconverter and sampler boards designed by Paul Horowitz for his SETI project. These accept an IF signal and yield I and Q complex samples with 8-bit precision.

To cover 10 MHz in two polarizations requires 16 Austek chips, or 16 FFT boards (4 chips/polarization x 2 polarizations x 2 for overlapped transforms). The data rate from *each* board is $R_{FFT} = 2mB$, where $B \leq 2.5$ MHz is the bandwidth, m is the number of bits per sample (in each of I and Q), and the factor of two allows for the complex nature of the output. Raw chip output is 16 bits (in each of I and Q). For searching, the MAC will take the squared magnitude, and a barrel shift will select the desired 8 bits. The data rate out of each MAC is $8B = 20 \text{ Mbits s}^{-1}$. For other analyses, where complex data are wanted, the data rate is twice this value. An accumulator on the FFT board allows a predetermined number of individual spectra to be summed, allowed values being in the range of 1 to 2^{18} , or $\sim 100\mu\text{s}$ to $\sim 26 \text{ s}$ for 256 point transforms. Accumulated spectra appear at the output port of each board, to be processed by an accumulator/packer board. At present, design of FFT boards is at a mature stage.

The accumulator/packer board accepts data streams from the 16 FFT boards and combines the data. This board is, at present, only at the conceptual stage. For searching, it should (1) subtract the mean spectrum from each data spectrum, the mean spectrum having been calculated and stored in a preliminary data run; (2) sum two hands of polarization; (3) select a small number of bits from the sum to be packed and shipped to a FIFO. If the sum of two polarizations is quantized to 2 bits, the net data rate so produced from a pair of boards is $2B$ bits s^{-1} . This sum may be combined with the sum from the pair of boards that calculates the 50% overlapped FFT (at the same RF) (the combining occurring before requantizing, of course). Thus 4 boards produce a rate of $2B$, so 16 boards yield $8B = 20 \text{ Mbits s}^{-1} = 2.5 \text{ Mbytes s}^{-1}$. Combining overlapped FFTs may be done in other ways, but they will generally yield the same reduction in data rate. This data rate is currently too large to be handled by recording systems at Arecibo, but efforts on data striping and other parallel recording methods eventually should be able to handle the data rate. Before that time, longer accumulation times and shorter FFT lengths can yield manageable data rates.

The downconverter/sampler boards along with LO sources will be packaged in a self-contained rack. FFT boards and the accumulator/packer board will reside in a VME crate. Output from this crate is expected to feed a digital input board on the new data acquisition system developed by Phil Perillat and Bill Sisk. Control of the system is via a serial port that may be driven by a dedicated computer or by the same computer that controls the Observatory's data acquisition system. These details are TBD.