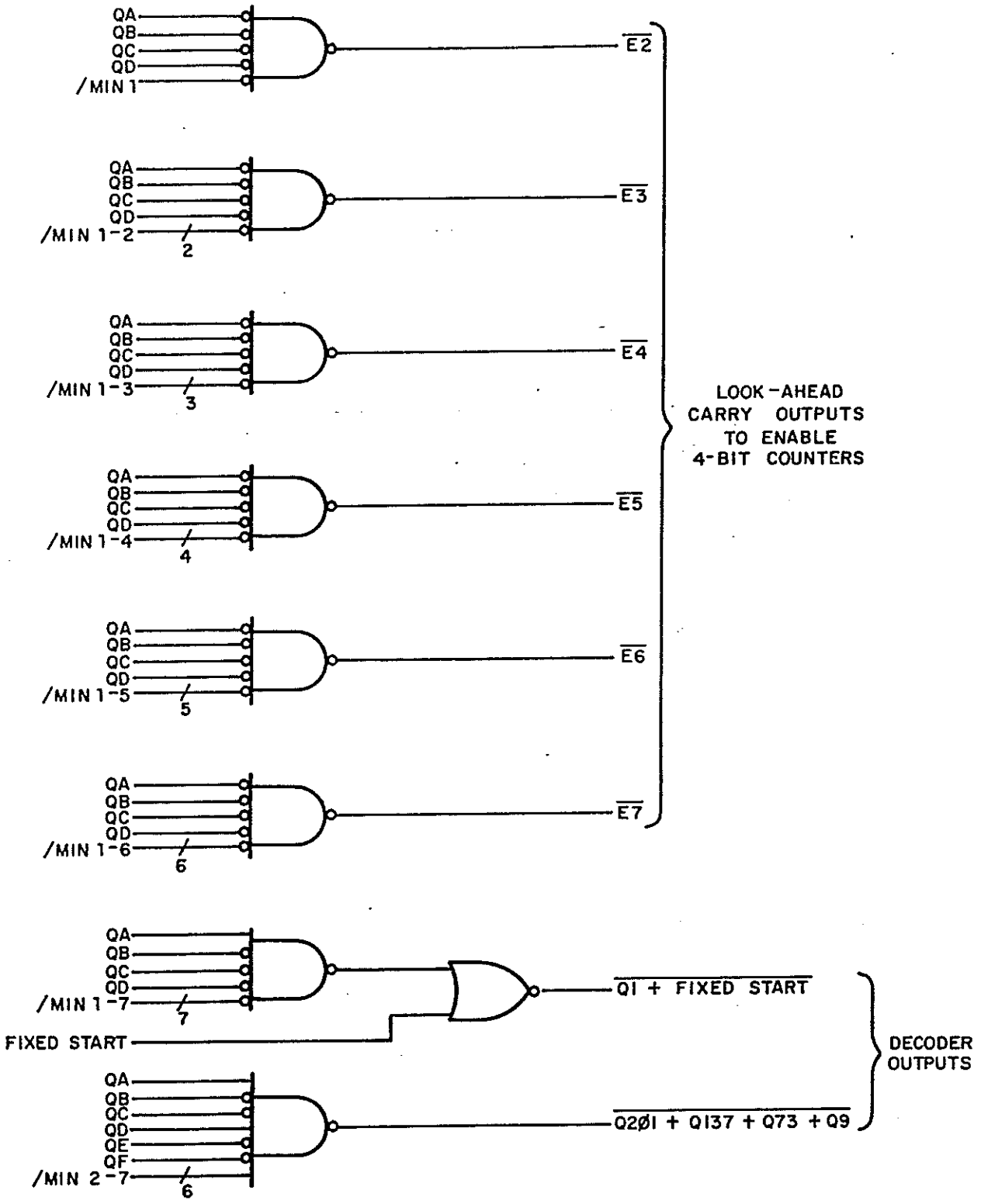
```
                    ;RTG/TS1 CODE (PALASM INPUT)

                    ;PAL CHIP USED IN TXIPP COUNTER


title       txippdec
pattern     ts1.pds
revision    a
author      ert
company     ao
date        5/22/87

chip        trippdec    pal2018

qa  qb  qc  qd  qe  qf  /min2  /min3  /min4/  min5  gnd
/min6  /min7  /E2  /E3  /E4  /E5  /E6  /E7  /Q1  /Q201 fixstart vcc

equations

E2 =  /qa * /qb * /qc * /qd * min1
E3 =  /qa * /qb * /qc * /qd * min1 * min2
E4 =  /qa * /qb * /qc * /qd * min1 * min2 * min3
E5 =  /qa * /qb * /qc * /qd * min1 * min2 * min3 * min4 * min5
E6 =  /qa * /qb * /qc * /qd * min1 * min2 * min3 * min4 * min5 * min6

                ; E2 to E7 are look-ahead carry outputs
                ; to enable 4-bit counters

Q1 = qa* /qb * /qc * min1 * min2 * min3 * min4 * min5 * min6 * min7 + fixstart

                ; decoder out (Q1=Q1+fixstart)

Q201 = qa * /qb * /qc * qd * /qe * /qf              ; decoder out
       min2 * min3 * min4 * min5 * min6 * min7      ; (Q201=Q201+Q137+Q73+Q9)
```

DWG. NO. D691C18A

USED IN TXIPP COUNTER
(PAL 20L8)

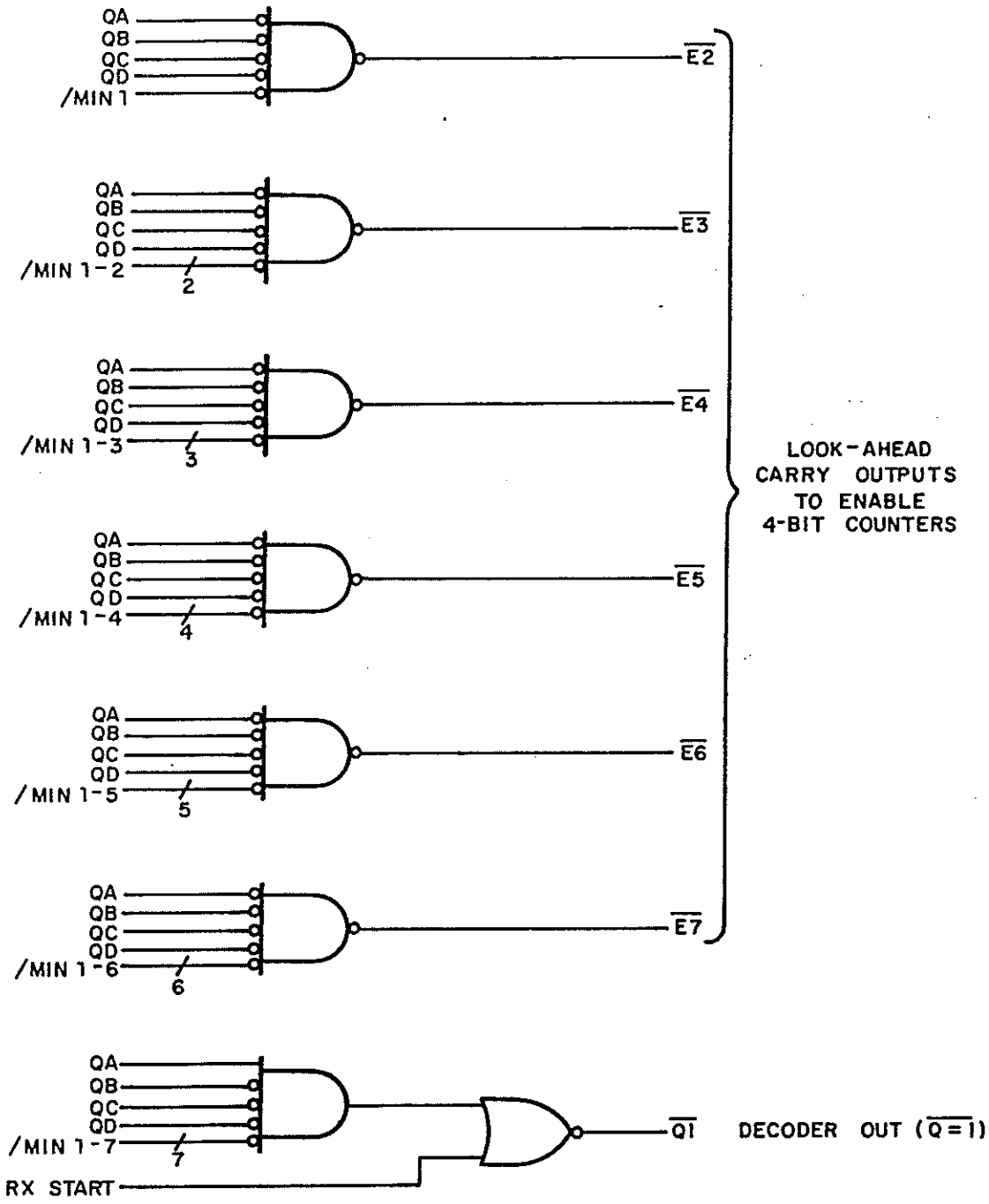


REVISIONS	DATE 4-20-89	ARECIBO OBSERVATORY CORNELL UNIVERSITY	SCALE
	APPD. E.R, TORRES	NAME TSI SCHEMATIC	DWN. NO. D691C18A0
	BY G.A. SERRANO		

```
                    ;RTG/TS2 CODE (PALAMS INPUT)

                    ;PAL CHIP USED IN RXIPP COUNTER


title       rxippdec
pattern     ts2.pds
revision    a
author      ert
company     ao
date        5/22/87

chip        rxippdec    pal2018

qa  qb  qc  qd /min1 /min2 /min3 /min4 /min5 /min6 /min7 gnd
rxstart nc /E2 /E3 /E4 /E5 /E6 /E7 nc /Q1 nc vcc

equations

E2 =  /qa * /qb * /qc * /qd * min1
E3 =  /qa * /qb * /qc * /qd * min1 * min2
E4 =  /qa * /qb * /qc * /qd * min1 * min2 * min3
E5 =  /qa * /qb * /qc * /qd * min1 * min2 * min3 * min4
E6 =  /qa * /qb * /qc * /qd * min1 * min2 * min3 * min4 * min5
E7 =  /qa * /qb * /qc * /qd * min1 * min2 * min3 * min4 * min5 * min6

                    ; E2 to E7 are look-ahead carry outputs
                    ; to enable 4-bit counters

Q1 = qa* /qb * /qc /qd * min1 * min2 * min3 * min4 * min5 * min6 * min7
     + rxstart

                    ; decoder out (Q1=Q1+rxstart)
```

DWG. NO. D691C19A0

RTG/TS2 DECODER
USED IN RXIPP COUNTER
(PAL 20L8)

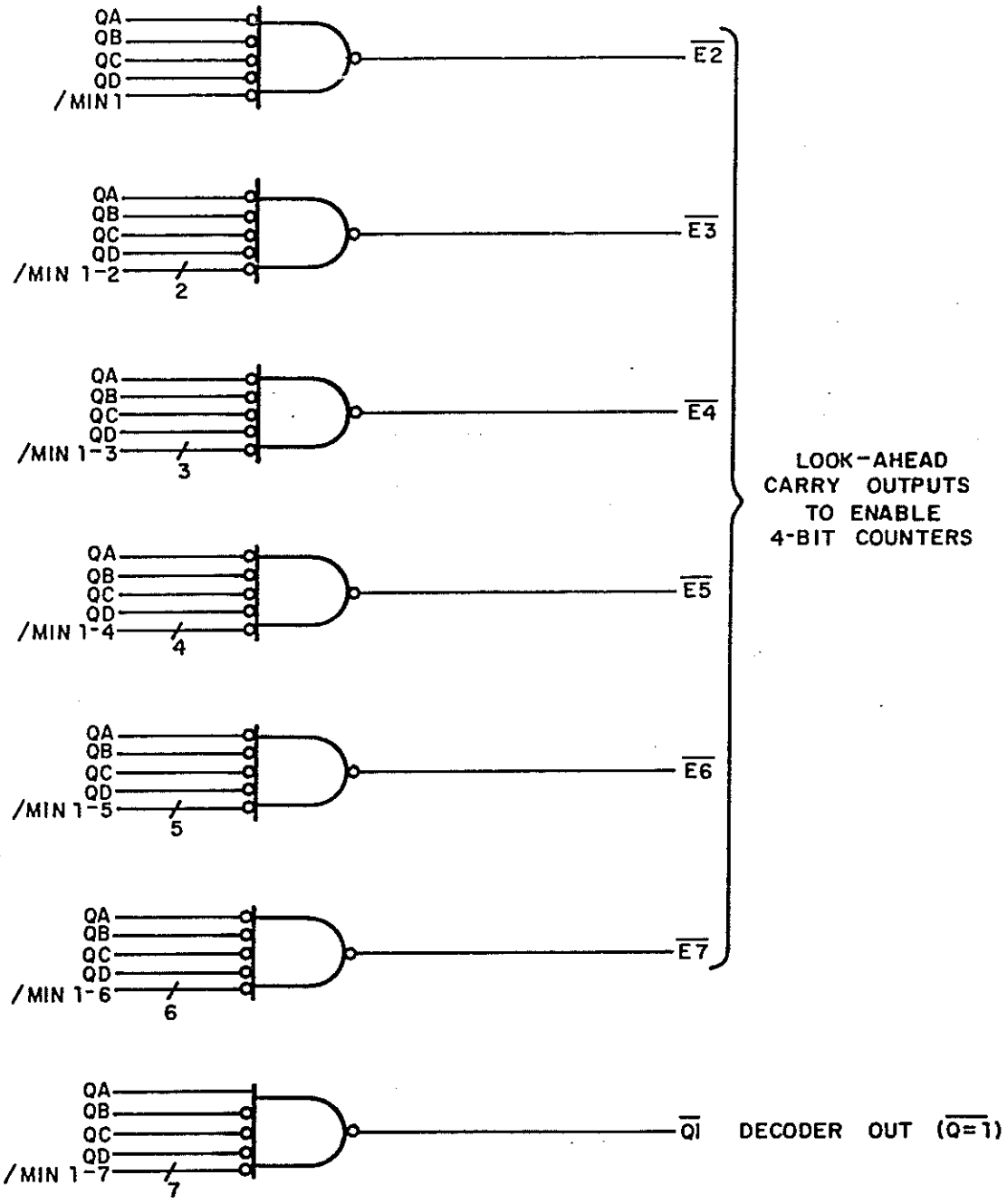


REVISIONS	DATE 4-20-89	ARECIBO OBSERVATORY CORNELL UNIVERSITY	SCALE
	APPD. E.R. TORRES	NAME TS2 SCHEMATIC	DWN. NO. D691C19A0
	BY G.A. SERRANO		

```
                    ;RTG/TS3 SOURCE CODE (PALAMS INPUT)

                    ;PAL CHIP USED IN GATE DELAY TIMER


title       gtedeldec
pattern     ts3.pds
revision    a
author      ert
company     ao
date        5/22/87

chip        gtedeldec   pal1618

qa  qb  qc  qd /min1 /min2 /min3 /min4 /min5 /min6 /min7 gnd
/min6 /Q1 /min7 /E2 /E3 /E4 /E5 /E6 /E7 vcc

equations

E2 =  /qa * /qb * /qc * /qd * min1
E3 =  /qa * /qb * /qc * /qd * min1 * min2
E4 =  /qa * /qb * /qc * /qd * min1 * min2 * min3
E5 =  /qa * /qb * /qc * /qd * min1 * min2 * min3 * min4
E6 =  /qa * /qb * /qc * /qd * min1 * min2 * min3 * min4 * min5
E7 =  /qa * /qb * /qc * /qd * min1 * min2 * min3 * min4 * min5 * min6

                    ; E2 to E7 are look-ahead carry outputs
                    ; to enable 4-bit counters

Q1 = qa* /qb * /qc /qd * min1 * min2 * min3 * min4 * min5 * min6 * min7

                    ; decoder out (Q1)
```

DWG. NO. D691C20A

RTG / TS3 DECODER
USED IN GATE DELAY TIMER
(PAL 16L8)

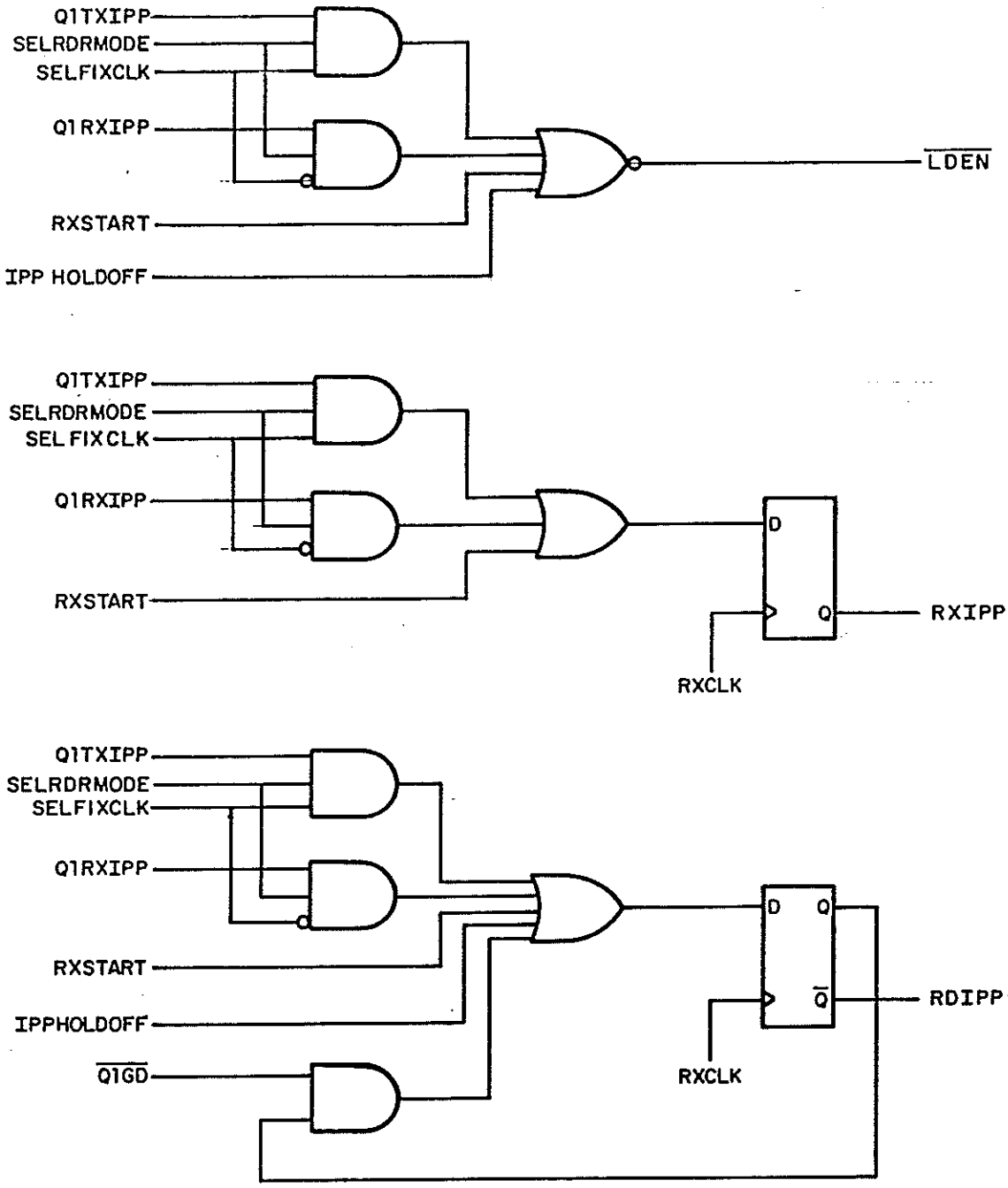


REVISIONS	DATE 4-26-89	ARECIBO OBSERVATORY CORNELL UNIVERSITY	SCALE
	APPD. E. R. TORRES	NAME TS3 SCHEMATIC	DWN. NO. D691C20A0
	BY G.A. SERRANO		

```
;RTG/TS4 SOURCE CODE (PALAMS INPUT)

;PAL CHIP USED IN GATE DELAY TIMER


title       gtedel-logic
pattern     ts4.pds
revision    a
author      ert
company     ao
date        5/22/87

chip        gtedel-logic      pal16r4


rxclk /qltxipp /qlrxipp /selfixclk rxstart ippholdoff selrdrmode /qlgd nc gnd
/oe nc nc nc nc /rxipp rdipptgr /lden nc vcc


equations

lden     := qltxipp * selrdrmode * selfixclk +       ; gate delay timer
            qlrxipp * selrdrmode * /selfixclk +      ; load enable
            rxstart * ippholdoff

rxipp    := qltxipp * selrdrmode * selfixclk +       ; this output is used
            qlrxipp * selrdrmode * /selfixclk +      ; as a front panel test
            rxstart                                  ; point only

/rdipptr:= qltxipp * selrdrmode * /selfixclk +       ; low during gate delay,
           qlrxipp * selrdrmode * /selfixclk +       ; rising edge triggers
           rxstart + ippholdoff + /qlgd * /rdipptgr  ; rdipp 100 us pulse,
                                                     ; high disables
                                                     ; gate delay timer
```

DWG. NO. D691C21A0

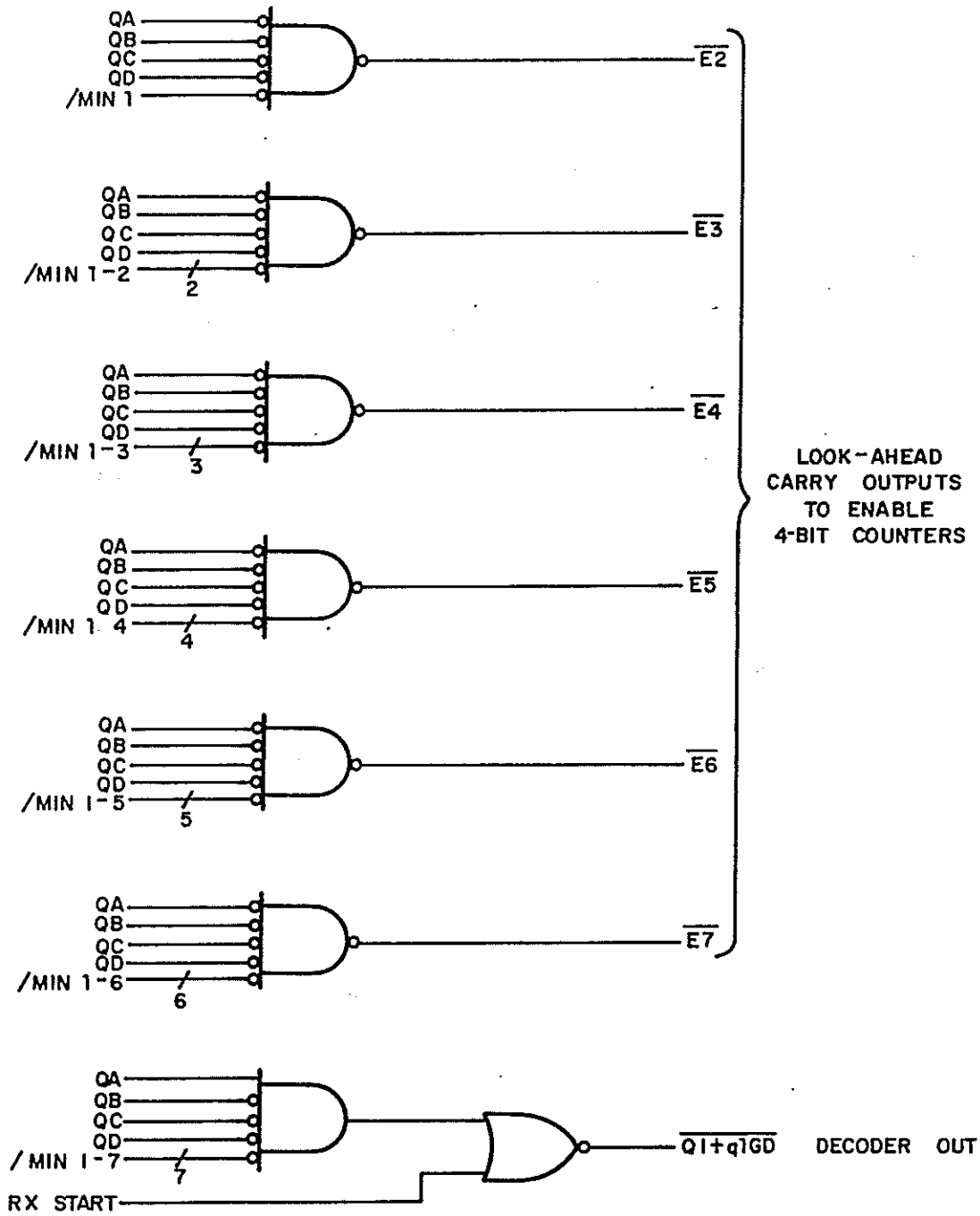
RTG/TS4 LOGIC
USED IN GATE DELAY TIMER
(PAL 16R4)



REVISIONS	DATE 4 - 26 - 89	ARECIBO OBSERVATORY CORNELL UNIVERSITY	SCALE
	APPD. E.R. TORRES	NAME TS4 SCHEMATIC	DWN. NO. D691C21A0
	BY G.A. SERRANO		

```
                    ;RTG/TS5 SOURCE CODE (PALASM INPUT)

                    ;PAL CHIP USED IN GATE WIDTH COUNTER


title       gtewthdec
pattern     ts5.pds
revision    a
author      ert
company     ao
date        5/22/87

chip        gtewthdec   pal2018


qa  qb  qc  qd /min1 /min2 /min3 /min4 /min5 /min6 /min7 gnd
nc /q1gd nc /E2 /E3 /E4 /E5 /E6 /E7 /Q1 nc vcc


equations

E2 =  /qa * /qb * /qc * /qd * min1
E3 =  /qa * /qb * /qc * /qd * min1 * min2
E4 =  /qa * /qb * /qc * /qd * min1 * min2 * min3
E5 =  /qa * /qb * /qc * /qd * min1 * min2 * min3 * min4
E6 =  /qa * /qb * /qc * /qd * min1 * min2 * min3 * min4 * min5
E7 =  /qa * /qb * /qc * /qd * min1 * min2 * min3 * min4 * min5 * min6

                    ; E2 to E7 are look-ahead carry outputs
                    ; to enable 4-bit counters

Q1 = qa * /qb * /qc /qd * min1 * min2 * min3 * min4 * min5 * min6 * min7
     + q1gd

                    ; decoder out (Q1=Q1+q1gd)
```

RTG /TS5 DECODER
USED IN GATE WIDTH
COUNTER (PAL 20L8)

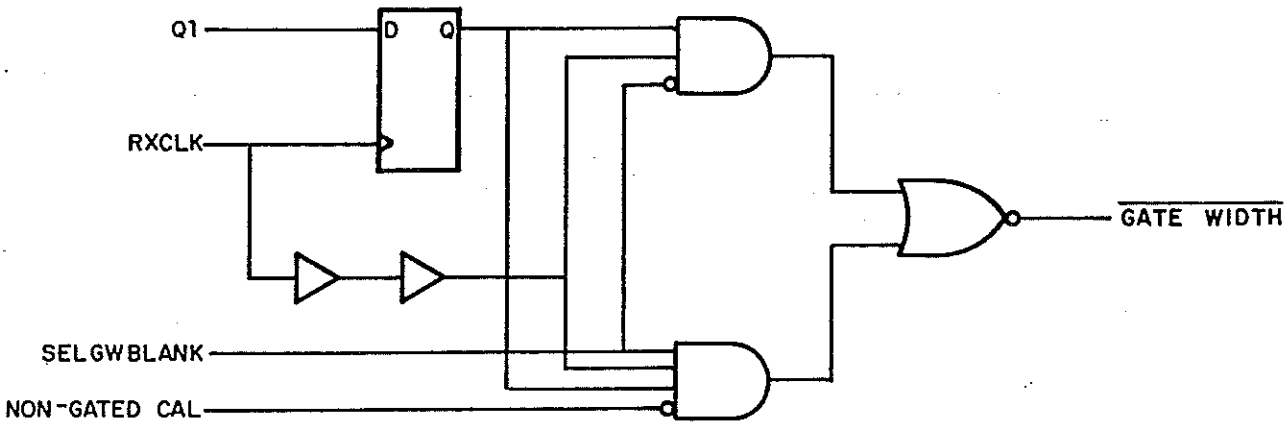


REVISIONS	DATE 4-27-89	ARECIBO OBSERVATORY CORNELL UNIVERSITY	SCALE
	APPD. E.R. TORRES	NAME TS5 SCHEMATIC	DWN. NO. D691C22A0
	BY G.A. SERRANO		

```
;RTG/TS6 SOURCE CODE (PALASM INPUT)

;PAL CHIP USED IN GATE WIDTH COUNTER


title       gtewth-logic
pattern     ts6.pds
revision    a
author      ert
company     ao
date        5/22/87

chip        gtewth-logic      pal16r4


clk /q1 rxclk selgwblank /ngcal nc nc nc nc gnd
/oe nc d30rxclk nc nc nc /en /d15rxclk /gw vcc


equations

en        :=  Q1                                    ; gate width load
                                                      enable (Q1) latched


d15rxclk   =  rxclk                                 ; rx clock delayed by
                                                      15 nanosec approximately

/d30rxclk  =  /d15rxclk                             ; rx clock delayed by
                                                      30 nanosec approximately

gw         =  en * d30rxclk * /selgwblank +         ; gate width input
              en * d30rxclk *  selgwblank * /ngcal
```

DWG. NO. D691C23A0

RTG/TS6 LOGIC
USED IN GATE WIDTH COUNTER
(PAL 16R4)

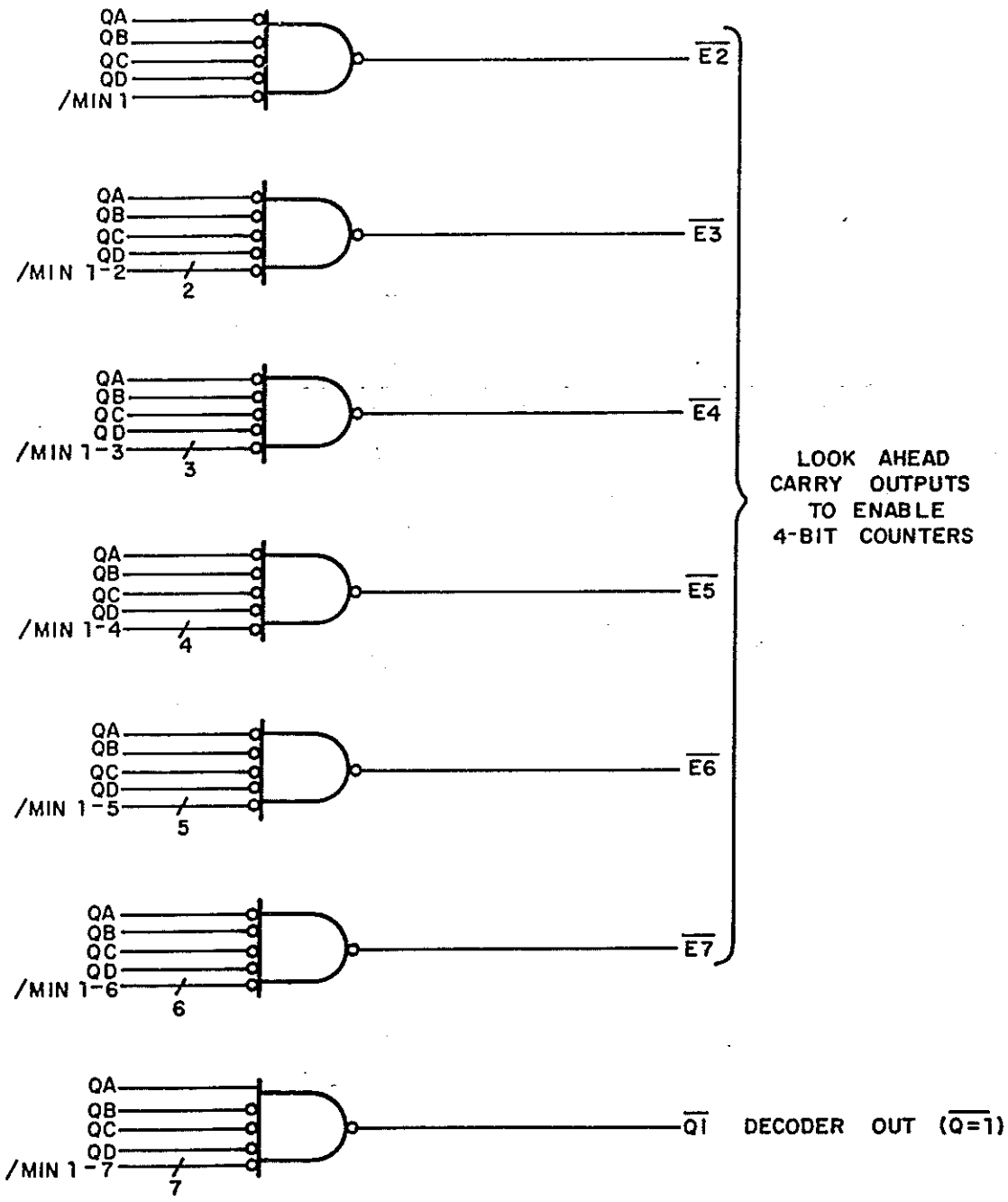


REVISIONS	DATE 4-27-89	ARECIBO OBSERVATORY CORNELL UNIVERSITY	SCALE
	APPD. E. R. TORRES	NAME TS6 SCHEMATIC	DWN. NO. D691C23A0
	BY G.A. SERRANO		

```
                    ;RTG/TS7 SOURCE CODE (PALASM INPUT)

                    ;PAL CHIP USED IN CAL DELAY TIMER


title       caldeldec
pattern     ts7.pds
revision    a
author      ert
company     ao
date        5/22/87

chip        caldeldec   pal1618


qa  qb  qc  qd /min1 /min2 /min3 /min4 /min5 gnd
/min6 /Q1 /min7 /E2 /E3 /E4 /E5 /E6 /E7 /Q1 vcc


equations

E2 =  /qa * /qb * /qc * /qd * min1
E3 =  /qa * /qb * /qc * /qd * min1 * min2
E4 =  /qa * /qb * /qc * /qd * min1 * min2 * min3
E5 =  /qa * /qb * /qc * /qd * min1 * min2 * min3 * min4
E6 =  /qa * /qb * /qc * /qd * min1 * min2 * min3 * min4 * min5
E7 =  /qa * /qb * /qc * /qd * min1 * min2 * min3 * min4 * min5 * min6

                    ; E2 to E7 are look-ahead carry outputs
                    ; to enable 4-bit counters

Q1 = qa * /qb * /qc /qd * min1 * min2 * min3 * min4 * min5 * min6 * min7

                    ; decoder out (Q1)
```

DWG. NO. D691C24A

RTG / TS7 DECODER
USED IN CAL DELAY TIMER
(PAL 16L8)

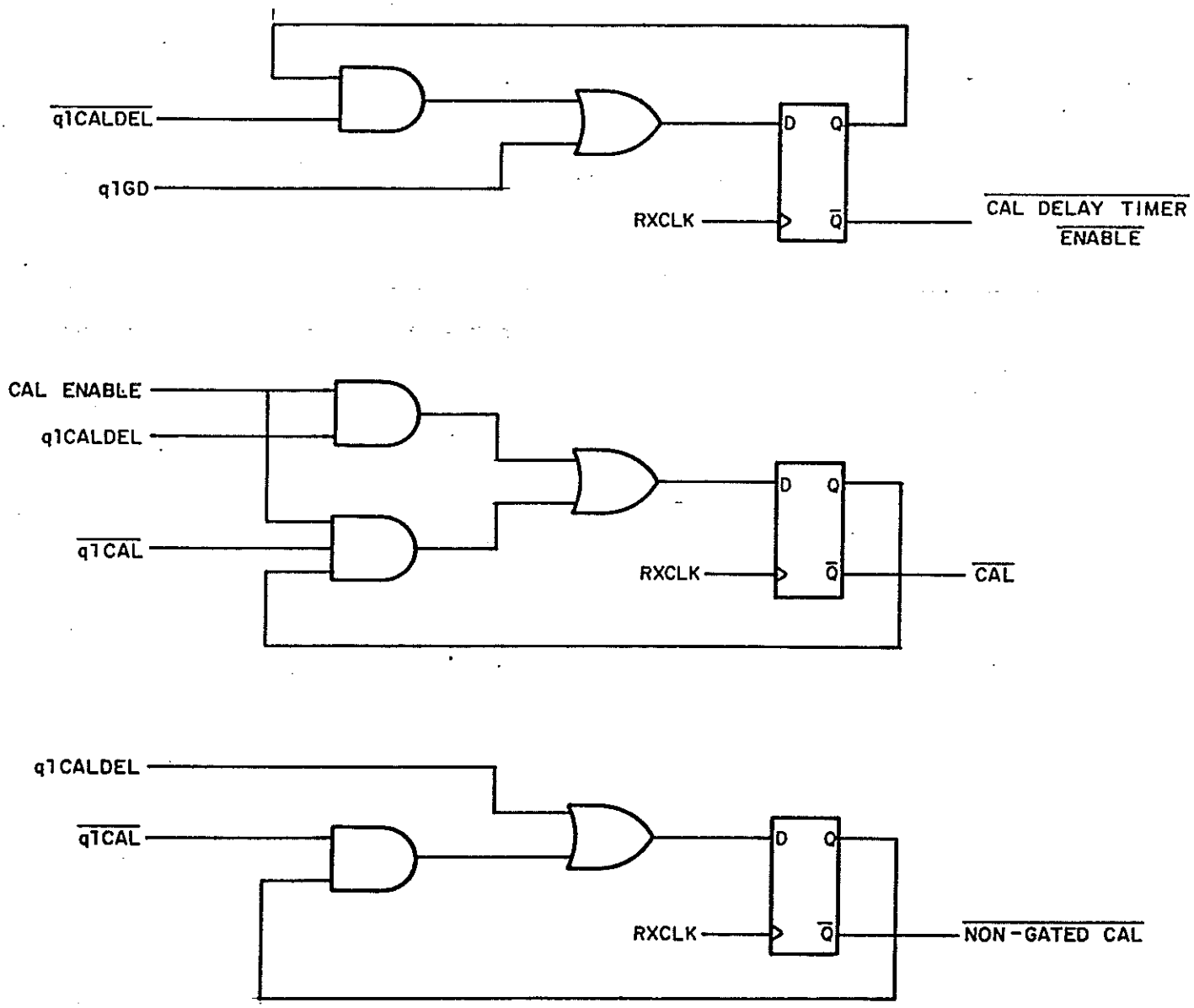


REVISIONS	DATE 4-27-89	ARECIBO OBSERVATORY CORNELL UNIVERSITY	SCALE
	APPD. E. R. TORRES	NAME TS7 SCHEMATIC	DWN. NO. D691C24A0
	BY G.A. SERRANO		

```
;RTG\TS8 SOURCE CODE (PALASM INPUT)

;PAL CHIP USED IN CAL DELAY & CAL WIDTH TIMERS


title       cal-logic
pattern     ts8.pds
revision    a
author      ert
company     ao
date        5-22-87


chip        cal-logic   pal16r4

rxclk /qlgd /qlcaldel /qlcal calenable nc nc nc nc gnd
/oe nc nc nc /ngcal /cal /cdt-en nc nc vcc


equations

cdt-en  :=  /qlcaldel * cdt-en + qlgd      ; cal delay timer enable
cal     :=  calenable * qlcaldel +         ; cal output
            calenable * /qlcal * cal

ngcal   :=  qlcaldel + /qlcal * ngcal      ; non-gated cal (same as cal
                                           ; but always enable)
```

DWG. NO. D691C25A0

RTG/TS8 LOGIC
USED IN CAL DELAY & WIDTH TIMERS
(PAL 16R4)

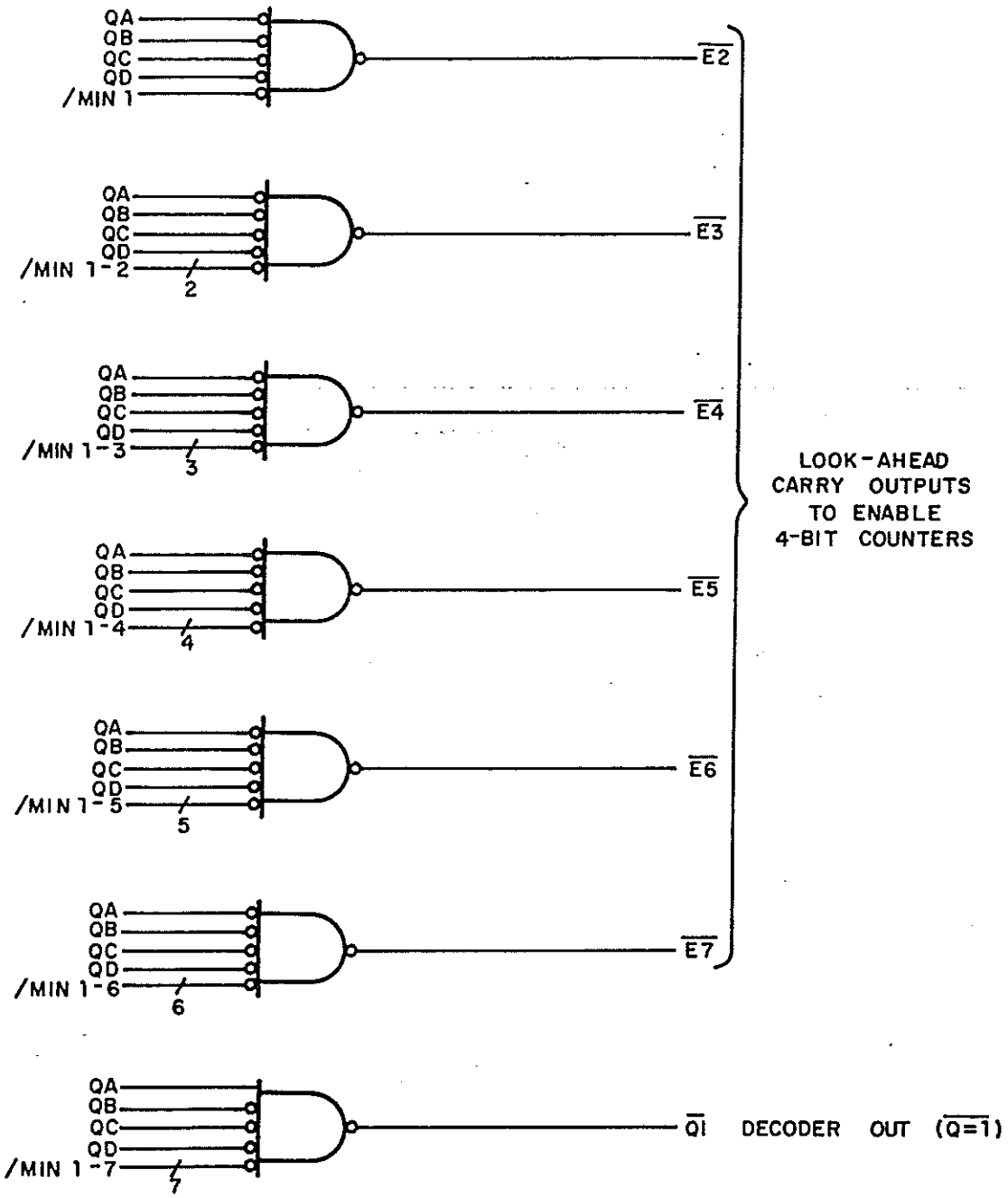


REVISIONS	DATE 4-27-89	ARECIBO OBSERVATORY CORNELL UNIVERSITY	SCALE
	APPD. E. R. TORRES	NAME TS8 SCHEMATIC	DWN. NO. D691C25A0
	BY G.A. SERRANO		

```
                    ;RTG/TS9 SOURCE CODE (PALASM INPUT)

                    ;PAL CHIP USED IN CAL WIDTH TIMER


title       calwthdec
pattern     ts9.pds
revision    a
author      ert
company     ao
date        5/22/87

chip        calwthdec   pal2018


qa  qb  qc  qd /min1 /min2 /min3 /min4 /min5 /min6 /min7 gnd
nc nc nc /Q1 /E2 /E3 /E4 /E5 /E6 /E7


equations

E2 =  /qa * /qb * /qc * /qd * min1
E3 =  /qa * /qb * /qc * /qd * min1 * min2
E4 =  /qa * /qb * /qc * /qd * min1 * min2 * min3
E5 =  /qa * /qb * /qc * /qd * min1 * min2 * min3 * min4
E6 =  /qa * /qb * /qc * /qd * min1 * min2 * min3 * min4 * min5
E7 =  /qa * /qb * /qc * /qd * min1 * min2 * min3 * min4 * min5 * min6

                    ; E2 to E7 are look-ahead carry outputs
                    ; to enable 4-bit counters

Q1 = qa * /qb * /qc /qd * min1 * min2 * min3 * min4 * min5 * min6 * min7

                    ; decoder out (Q1)
```

DWG. NO. D691C26A

RTG / TS9 DECODER
USED IN CAL WIDTH TIMER
(PAL 20L8)

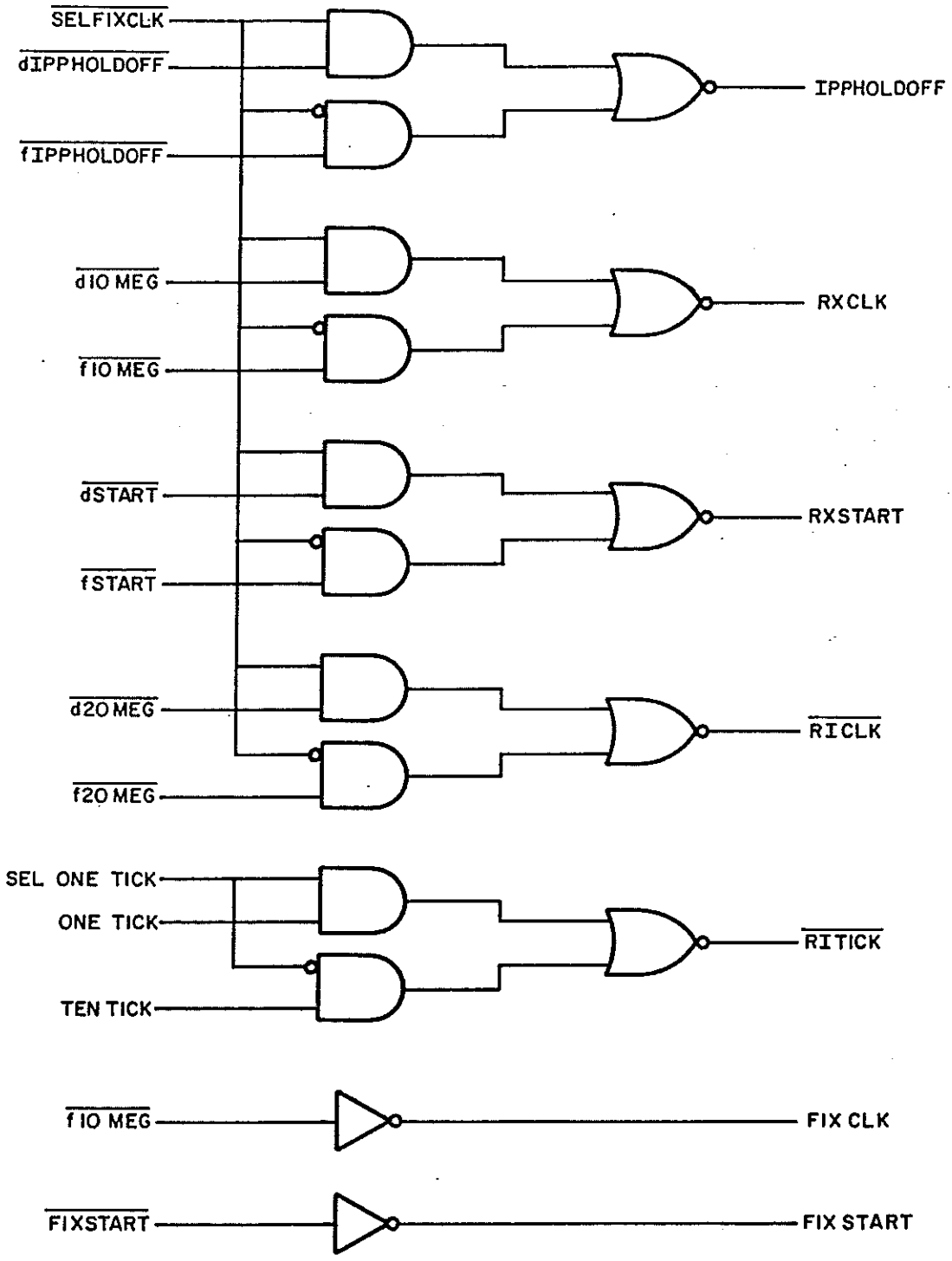


REVISIONS	DATE 4-28-89	ARECIBO OBSERVATORY CORNELL UNIVERSITY	SCALE
	APPD. E. R. TORRES	NAME TS9 SCHEMATIC	DWN. NO. D691C26A0
	BY G.A. SERRANO		

```
;RTG/TS10 SOURCE CODE (PALASM INPUT)

;PAL CHIP USED IN THE CLOCK CONDITIONER MUX


title       clk-cond-mux
pattern     ts10.pds
revision    a
author      ert
company     ao
date        5-22-87


chip        clk-cond-mux      pal2018


/fippholdoff /dippholdoff /f10meg /d10meg /fstart /dstart
/f20meg /d20meg tentick onetic /selfixclk gnd
selonetick nc rxstart nc /ritick /riclk rxclk fixclk
ippholdoff fixstart nc vcc


equations

/ippholdoff =  /fippholdoff * selfixclk +     ; ippholdoff,
               /dippholdoff * /selfixclk      ; fixed or drifted

/fixclk     =  /f10meg                        ; 10 MHz fixed clock

/rxclk      =  /f10meg * selfixclk +          ; 10 MHz rx clock,
               /d10meg * /selfixclk           ; fixed or drifted

/fixstart   =  /fstart                        ; fixed 100 nanosec
                                              ; start pulse

/rxstart    =  /fstart * selfixclk +          ; rx 100 nanosec start pulse,
               /dstart * /selfixclk           ; fixed or drifted

riclk       =  /f20meg * selfixclk +          ; radar interface 20 MHz
               /d20meg * /selfixclk           ; clock output,
                                              ; fixed or drifted

ritick      =  onetick * selonetick +         ; radar interface one sec
               tentick * /selonetick          ; or ten sec tick output
```

DWG. NO. D691C27A0

RTG/TSIO 2:1 MUX
USED IN CLOCK CONDITIONER
(PAL 20L8)

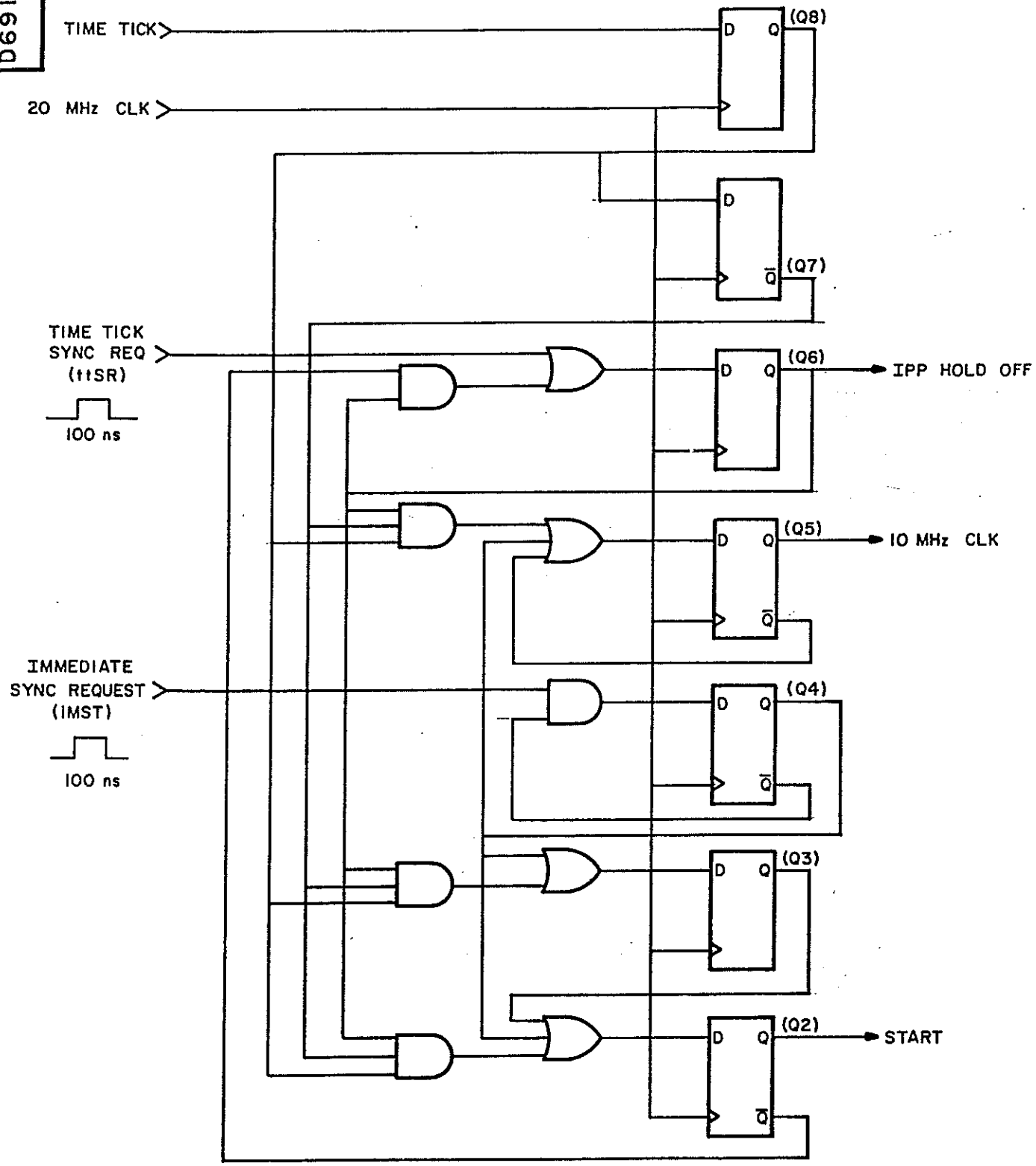


REVISIONS	DATE 4-28-89	ARECIBO OBSERVATORY CORNELL UNIVERSITY	SCALE
	APPD. E.R. TORRES	NAME TSIO SCHEMATIC	DWN. NO. D691C27A0
	BY G.A. SERRANO		

```
                    ;RTG/TS11 SOURCE CODE (PALASM INPUT)

                    ;PAL CHIP USED IN CLOCK CONDITIONER


title       clk-sync
pattern     ts11.pds
revision    a
author      ert
company     ao
date        5-22-87


chip        clk-sync    pal16r8

clk ttin ttsr imst nc nc nc nc nc gnd
/oe /start nc /q3 /q4 /clkout /ippholdoff /q7 /q8 vcc

equations

q8          := ttin                                 ;synchronized time tick

q7          := q8                                   ;delayed time tick (50 ns)

ippholdoff := ttsr + /start * ippholdoff            ;ippholdoff turns on with
                                                    ;a time tick sync request,
                                                    ;and turns off with the
                                                    ;start pulse

clkout      := /clkout + q4 + q8 * /q7 * ippholdoff ;10MHz clock synchronized
                                                    ;with a time tick sync req
                                                    ;(q8*/q7*ippholdoff)
                                                    ;or an immediate sync req
                                                    ;(q4)

q4          := imst * /q4                           ;immediately start(sync)
                                                    ;req latched

q3          := q4 + q8 * /q7 * ippholdoff           ;keep alive start pulse
                                                    ;(see next comment)

start       := q3 + q4 + q8 * /q7 * ippholdoff      ;start pulse generated by
                                                    ;a time tick sync req or
                                                    ;an immediate synch req &
                                                    ;keep alive for an extra
                                                    ;clock (50 nanosec) by q3
                                                    ;total duration = 100 ns
```

DWG. NO. D691C28A

USED IN CLOCK CONDITIONER
(PAL 16R8)

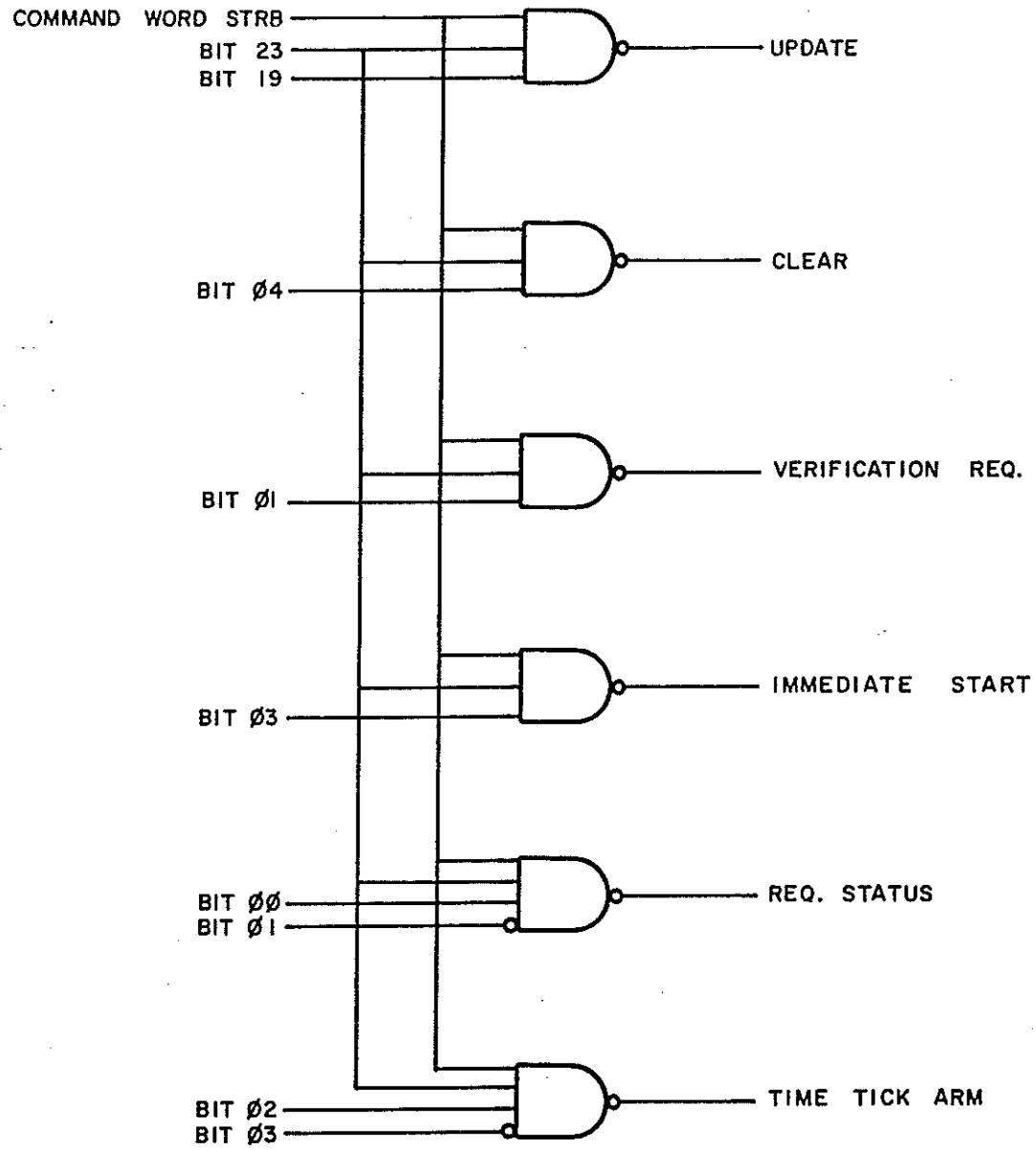


REVISIONS	DATE 4-28-89	ARECIBO OBSERVATORY CORNELL UNIVERSITY	SCALE
	APPD. E.R. TORRES	NAME TSII SCHEMATIC	DWN. NO. D691C28A0
	BY G.A. SERRANO		

```
                ;RTD/TS12 SOURCE CODE (PALASM INPUT)

                ;PAL CHIP USED IN THE INTERFACE


title       cmmnd-word-dec
pattern     ts12.pds
revision    a
author      ert
company     ao
date        5-22-87

chip        cmmnd-word-dec-pal1618


bit00  bit01 bit02  bit03 bit04 bit19 bit23 /cmmndwordstrb nc gnd
nc /clr /immstart /timetickarm /reqstatus /verifreq nc nc /update vcc

equations

update     = /cmmndwordstrb * bit23 * bit19          ;bit 19
                                                     ;  0 nop
                                                     ;  1 update parameters

clr        = /cmmndwordstrb * bit23 * bit 04         ;bit 4
                                                     ;  0 nop
                                                     ;  1 clear error flags

reqstatus  = /cmmndwordstrb * bit23 * bit 00* /bit01 ;bit 1,0
                                                     ;   00 nop
verifreq   = /cmmndwordstrb * bit23 * bit 01         ;   01 status request
                                                     ;   1x verification req

timetickarm= /cmmndwordstrb * bit23 * bit02 * /bit03 ;bit 3,2
                                                     ;  00 nop
immstart   = /cmmndwordstrb * bit23 * bit03          ;  01 time tick arm
                                                     ;  1x immediate start
```

DWG. NO. D691C29A0

RTG/TSI2
COMMAND WORD DECODER
USED IN THE INTERFACE
(PAL 16L8)

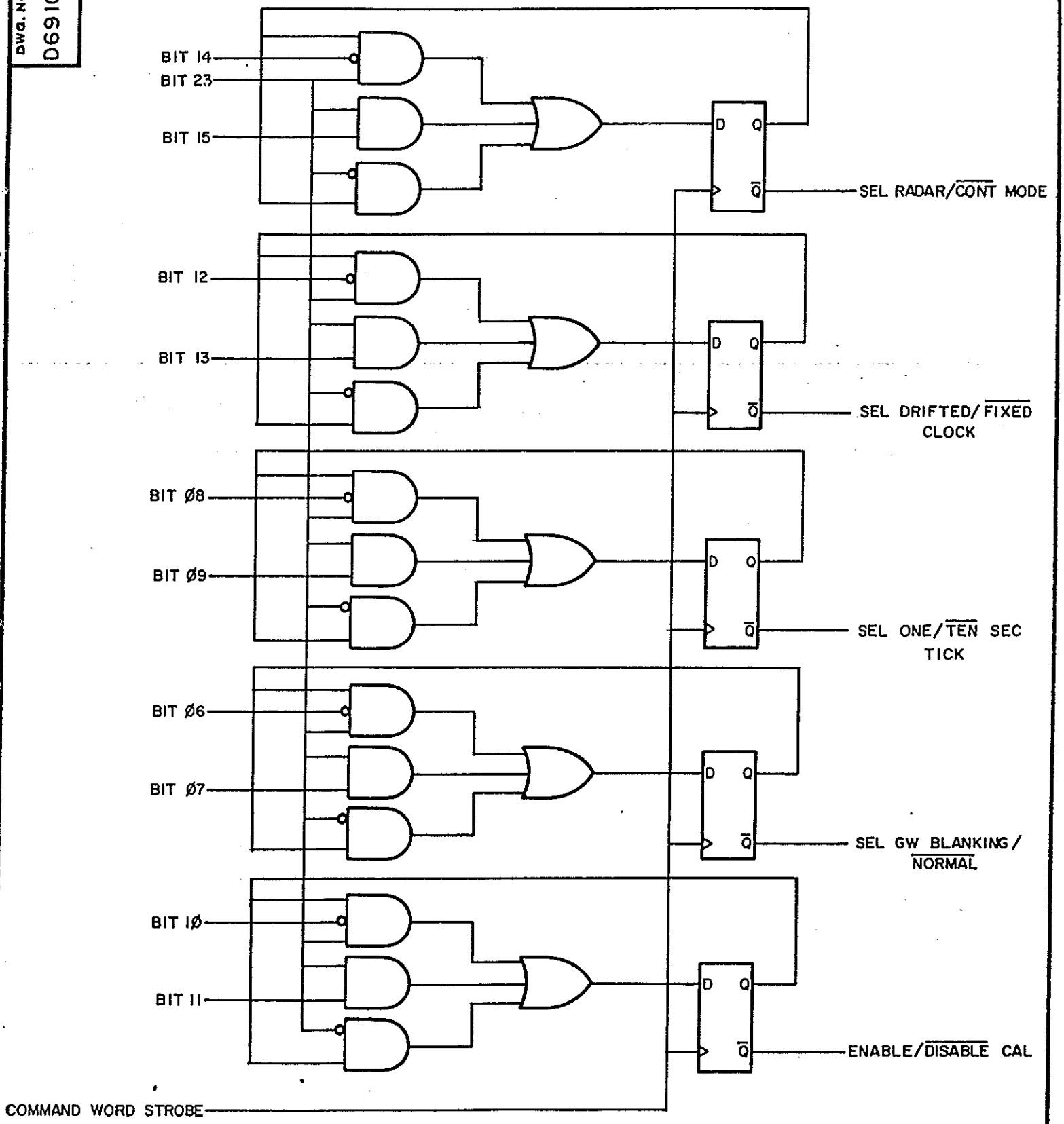


REVISIONS	DATE 4 - 28 - 89	ARECIBO OBSERVATORY CORNELL UNIVERSITY	SCALE
	APPD. E.R. TORRES	NAME TSI2 SCHEMATIC	DWN. NO. D691C29A0
	BY G.A. SERRANO		

```
;RTD/TS13 SOURCE CODE (PALASM INPUT)

;PAL CHIP USED IN THE INTERFACE


title       cnt-word-latch
pattern     ts13.pds
revision    a
author      ert
company     ao
date        5-22-87

chip        cnt-word-latch-pal20r8


/cmmndwordstrb bit06  bit07 bit08  bit00 bit10 bit11 bit12 bit13 bit14 bit15
gnd /oe bit23 rdr-cont-mode drift-fix-clk en-dis-cal one-ten-tick gw-blank-
norm nc nc nc nc vcc

equations

/rdr-cont-mode := rdr-cont-mode * /bit14 * bit23  ;bit 15, 14
                  bit15 * bit23 +                 ; 00 nop
                  rdr-cont-mode * /bit23          ; 01 radar sampling mode
                                                  ; 1x cont sampling mode

/drift-fix-clk := drift-fix-clk * /bit12 * bit23+ ;bit 13, 12
                  bit13 * bit23 +                 ; 00 nop
                  drift-fix-clk * /bit23          ; 01 sel drifted clock
                                                  ; 1x sel fixed clock

/en-dis-cal    := en-dis-cal * /bit10 * bit23 +   ;bit 11, 10
                  bit11 * bit23                   ; 00 nop
                  en-dis-cal * /bit23             ; 01 enable cal out
                                                  ; 1x disable cal out

/one-ten-tick  := one-ten-tick * /bit08 * bit23+  ;bit 8, 8
                  bit 09 * bit23 +                ; 00 nop
                  one-ten-tick * /bit23           ; 01 sel one sec tick
                                                  ; 1x sel ten sec tick

/gw-blank-norm := gw-blank-norm * /bit06 * bit23+ ;bit 7, 6
                  bit07 * bit23 +                 ; 00 nop
                  gw-blank-norm * /bit23          ; 01 gate width blank
                                                  ; 1x gate width normal
```

DWG. NO. D691C30A

COMMAND WORD LATCH USED IN THE INTERFACE
(PAL 20R8)



REVISIONS	DATE 5 - 1 - 89	ARECIBO OBSERVATORY CORNELL UNIVERSITY	SCALE
	APPD. E. R. TORRES	NAME TS13 SCHEMATIC	DWN. NO. D691C30A0
	BY G.A. SERRANO		

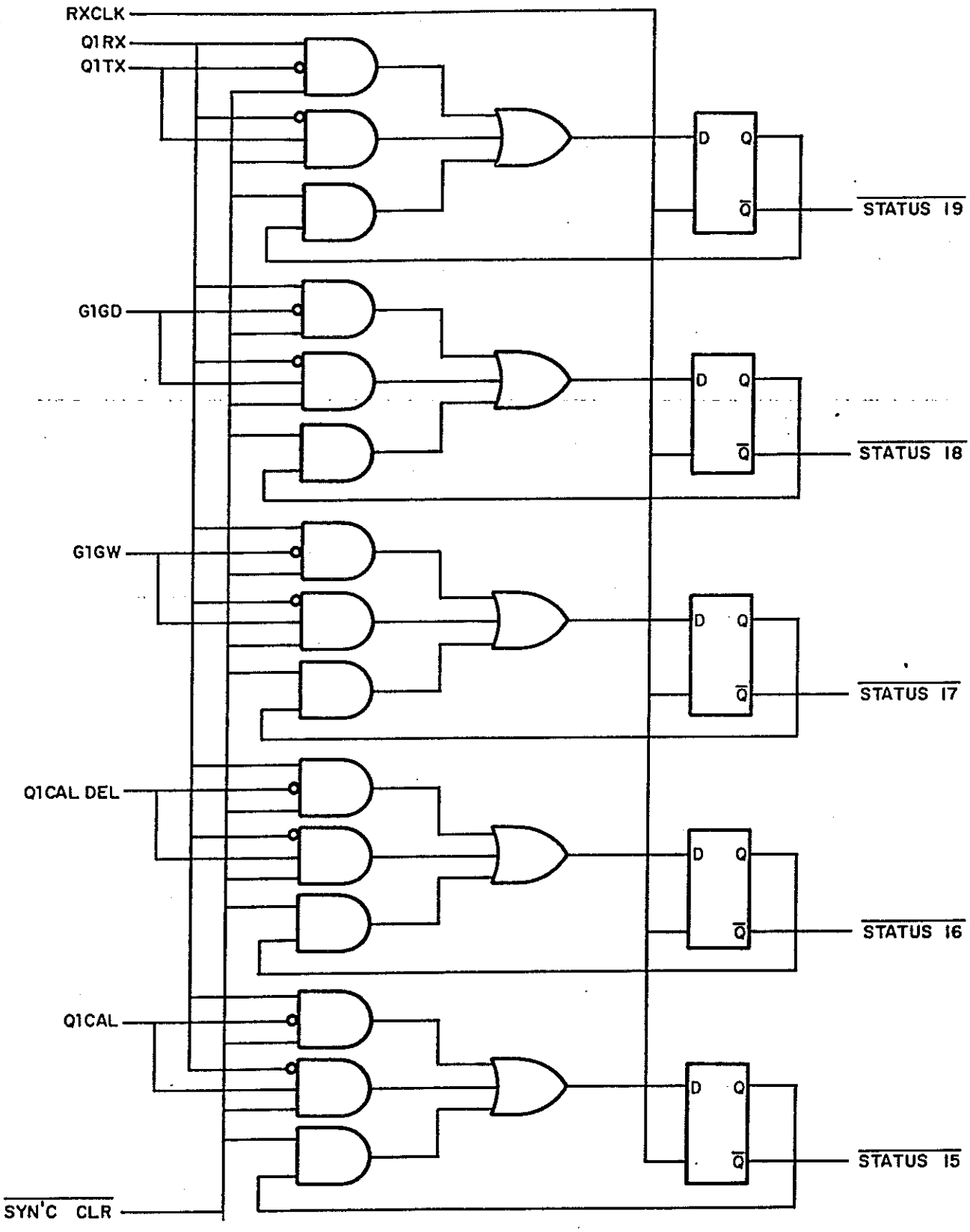
```
;RTG/TS14 SOURCE CODE (PALASM INPUT)

;PAL CHIP USED IN THE TIMING TEST COMPARATOR


title       ttc
pattern     ts14.pds
revision    a
author      ert
company     ao
date        5-22-87

chip        ttc         pal16r6


rxclk /qltxipp /qlrxipp /qlgd /qlgw /qlgw /qlcakdel /qlcal /clr nc gnd
/oe nc st19 st18 st17 st15 nc nc vcc

equations

/st19 :=  qlrxipp * /qltxipp * /clr +                ;status 19 =
          /qlrxipp * qltxipp * /clr + /st19 * /clr   ;qlrxipp exor qltxipp

/st18 :=  qlrxipp * /qlgd * /clr +                   ;status 18 =
          /qlrxipp * glgd * /clr + /st18 * /clr      ;qlrxipp exor qlgd

/st17 :=  qlrxipp * /qlgw * /clr +                   ;status 17 =
          /qlrxipp * qlgw * /clr + /st17 * /clr      ;qlrxipp exor qlgw

/st16 :=  qlrxipp * /qlcaldel * /clr +               ;status 16 =
          /qlrxipp * qlcaldel * /clr + /st16 * /clr  ;qlrxipp exor qlcd

/st15 ;=  qlrxipp * /qlcal * /clr +                  ;status 15 =
          /qlrxipp * qlcal * /clr + /st15 * /clr     ;qlrxipp exor qlcal

      ;note that the clear is syncronous
```

DWG. NO. D691C31A0

RTG/TS14

LOGIC USED IN THE TIMING TEST COMPARATOR

(PAL 16R6)



REVISIONS	DATE 5 - 1 - 89	ARECIBO OBSERVATORY CORNELL UNIVERSITY	SCALE
	APPD. E. R. TORRES	NAME TS14 SCHEMATIC	DWN. NO. D691C31A0
	BY G.A. SERRANO		

INSTRUCTION MANUAL

REGULATED POWER SUPPLIES

LUS-10A SERIES

1 SPECIFICATIONS

	Items \ Model		LUS-10A-5	LUS-10A-6	LUS-10A-9	LUS-10A-12	LUS-10A-15	LUS-10A-18	LUS-10A-24	LUS-10A-28
1	Nominal Output Voltage	V	5	6	9	12	15	18	24	28
2	Maximum Output Current	A	10.0	8.4	5.6	4.2	3.4	2.8	2.1	1.8
3	Maximum Output Power	W	50.0	50.4	50.4	50.4	51.0	50.4	50.4	50.4
4	Efficiency (Typ) (•1)	%	70	70	73	76	76	78	80	80
5	Input Voltage Range	—	85~132VAC(47~440Hz) or 110~165VDC							
6	Input Current (Typ) (•1)	A	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
7	In-rush Current (Typ) (•2)	A	10A at 100VAC (130VDC)							
8	Output Voltage Range (Typ)	%	±5%							
9	Maximum Ripple & Noise	mV	120	120	150	150	150	150	200	200
10	Maximum Line Regulation (•3)	%	0.4							
11	Maximum Load Regulation (•4)	%	0.85							
12	Over Current Protection (•5)	A	10.5~14.0	8.80~11.8	5.80~7.80	4.40~5.80	3.60~4.80	3.00~4.00	2.20~3.00	1.90~2.60
13	Over Voltage Protection (•6)	V	5.65~6.40	6.90~8.00	10.6~12.0	13.8~15.6	17.3~20.0	20.7~24.3	27.6~32.4	32.2~37.8
14	Hold-Up Time (•7)	mS	More than 16mS							
15	Remote Sensing	—	—							
16	Remote ON/OFF Control	—	—							
17	Parallel Operation	—	—							
18	Series Operation	—	Possible							
19	Operating Temperature (•8)	°C	0 ~ +60°C							
20	Operating Humidity	%	30% ~ 90% RH							
21	Storage Temperature	°C	-30 ~ +85°C							
22	Storage Humidity	%	10% ~ 95% RH							
23	Cooling	—	Convection cooled							
24	Temperature Coefficient (Typ)	%	1% at 0°C ~ +60°C							
25	Withstand Voltage (•9)	kV	Inout-Chassis, Inout-Outout ···1.5KVAC 1MIN							
26	Isolation Resistance	Ω	More than 60 MΩ at 25°C and 70%RH Output-Chassis ···500VDC							
27	Vibration	G	Less than 2G							
28	Shock	G	Less than 20G							
29	Weight	g	425							
30	Size	—	Refer to Outline Drawing							
31	Finish	—	Gray, FED, STD, 595 No. 26081							

NOTES

- •1 : At100VAC & Maximum output power.
- •2 : When resuming operation in less than 5 sec after power failure at no load, softstart circuit will not limit the in-rush current at turn-on.
- •3 : From 85~132VAC, constant load.
- •4 : From No load ~ Full load, constant input voltage.
- •5 : Constant current limiting with automatic recovery.
- •6 : Inverter shut-down method, manual reset.
- •7 : At 100VAC, Nominal output voltage & Maximum output current.
- •8 : Ratings : Percent of Maximum output current or Maximum output power, Whichever is greater.
  0 ~ 50°C ··· 100% , 60°C ··· 50%
  0 ~ 50°C ··· 100% , 60°C ··· 70% (Forced air required)
- •9 : Leakage current range used : Input-Chassis, Input-Output greater than 20mA

1302 - 4 - 132 PRINTED IN JAPAN

INPUT POWER —73 watts maximum with output loaded to full current rating and input voltage 132 volts AC at 60 Hz.

INPUT FUSE —Fuse F1, 4A Slo-Blo, in AC input line protects the input wiring to the power supply. Overload of power supply does not cause fuse failure.

INPUT AND OUTPUT CONNECTIONS —See Outline Drawing for location. Terminal block on front of chassis contains all terminals for AC input, DC output and ground connections.

OVERSHOOT —No overshoot under conditions of power turn-on, turn-off or power failure.

DC OUTPUT CONTROL —Screwdriver voltage adjust control permits adjustment of DC output voltage. See Outline Drawing for location of control.

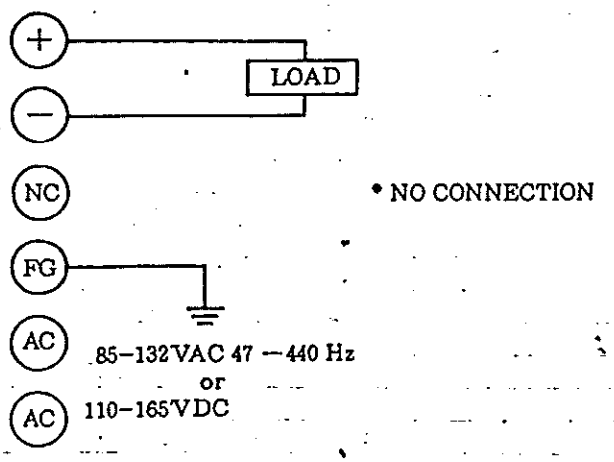
OUTPUT STATUS INDICATOR —L.E.D. light indicates presence of output voltage.

GUARANTEE —1 year guarantee from date of shipment ..... materials and labor.

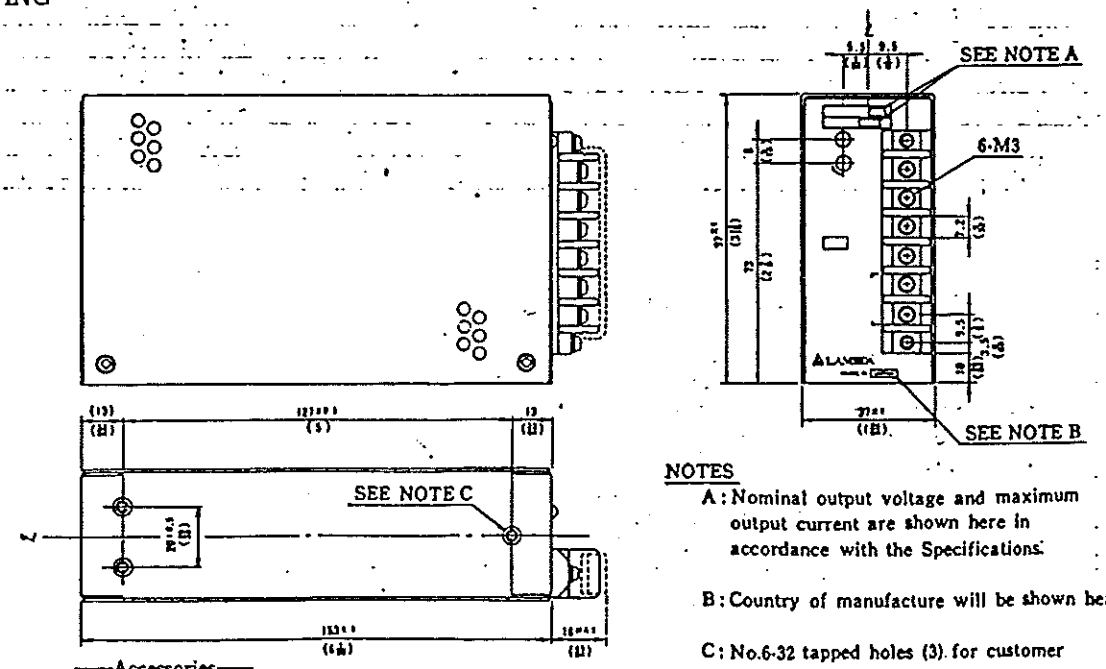
MOUNTING—One surface with threaded mounting holes can be utilized for mounting this unit. Air circulation is required when unit is mounted in confined areas. Refer to Outline Drawing for mounting details.

OVERVOLTAGE PROTECTION —Internally mounted Overvoltage Protectors are provided as standard equipment on all models.

II DC OUTPUT CONNECTION DIAGRAM



III OUTLINE DRAWING



—Accessories—
Cover for barrier terminal strip.
(Mounted on terminal strip at time of shipment.)

NOTES

A : Nominal output voltage and maximum output current are shown here in accordance with the Specifications.

B : Country of manufacture will be shown here.

C : No.6-32 tapped holes (3) for customer chassis mounting.
[Screws must not protrude into P.S. by more than 6⅝. (4.5)]

9.0 GLOSSARY

Cal — The output used to turn on a receiver calibration source. Used for on-line system performance monitoring.

Continuous Mode:
Only one RDIPP is produced after a start command. The gatewidth pulse train is synchronized to this single RDIPP and thereafter runs continuously. The Cal output remains LO.

Drifted Clock:
A 10 MHz internal clock derived from the (nearly) 20 MHz drifted clock input.

Fixed Clock:
A fixed 10 MHz internal clock derived from the 20 MHz fixed clock input.

Gate Delay:
Delay between the transmitter pulse and the RDIPP. Also, for continuous sampling, the delay between the start tick and the commencement of sampling.

Gatewidth Blanking:
Gate width pulses are blanked during the cal pulse interval.

GW — Gatewidth - the sampling pulses sent to the RI.

Radar Mode:
The gatewidth pulse train is restarted (resynchronized) at every RDIPP.

RDIPP — Delayed RECEIVER IPP - framing pulse sent to the RI.

RI — Radar Interface

RMUX — Radar Multiplexer

RTG — Radar Timing Generator

TXIPP — The RTG output that triggers the 430 MHz transmitter.

INDEX

NOTES