**8.1 RIPAL00**

```
;PALASM Design Description

;---------- Declaration Segment ----------
TITLE       RIPAL00.PDS
PATTERN     VME RADAR INTERFACE 16-BIT PACKER, 1-4 OF 4 CHIPS
REVISION    0
AUTHOR      BILL SISK
COMPANY     ARECIBO OBSERVATORY
DATE        11/5/92

CHIP  RIPAL00  PAL20V8

;---------- PIN Declarations ----------
PIN  24      VCC
PIN  12      GND
PIN  1       CLK          COMB ; INPUT
PIN  2..5    A[3..0]      COMB ; INPUT
PIN  18..21  Q[0..3]      REG  ; OUTPUT
PIN  15..17  P[0..2]      COMB ; INPUT

;---------- Boolean Equation Segment ----
EQUATIONS

CASE (P[2..0])
      BEGIN
      #b000:                    ;16 BIT PACKING W/ SIGN EXTENSION
            BEGIN
             Q[3..0] = A[3]
      END
      #b001:                    ;8 BIT PACKING
            BEGIN
            Q[3..0] = A[3..0]
            END
      #b010:                    ;4 BIT PACKING
            BEGIN
            Q[3..0] = A[3..0]
            END
      #b011:                    ;2 BIT PACKING
            BEGIN
            Q[3..2] = A[3..2]
            Q[1..0] = Q[3..2]
            END
```

```
#b111:                  ;1 BIT PACKING
        BEGIN
         Q[3] = A[3]
         Q[2..0] = Q[3..1]
        END
OTHERWISE:              ;UNUSED CASES DEFAULT TO O
        BEGIN
         Q[3..0] = 0
        END
END
```

## 8.2 RIPAL01

```
;PALASM Design Description

;———————— Declaration Segment ————————
TITLE       RIPAL01.PDS
PATTERN     VME RADAR INTERFACE 16-BIT PACKER, 2-4 OF 4 CHIPS
REVISION    0
AUTHOR      BILL SISK
COMPANY     ARECIBO OBSERVATORY
DATE        11/5/92

CHIP  RIPAL01  PAL20V8

;———————— PIN Declarations ————————————-
PIN  24              VCC
PIN  12              GND
PIN  1               CLK          COMB ; INPUT
PIN  2..5            A[3..0]      COMB ; INPUT
PIN  6..9            B[3..0]      COMB ; INPUT
PIN  10,11,22,23     C[3..0]      COMB ; INPUT
PIN  18..21          Q[0..3]      REG  ; OUTPUT
PIN  15..17          P[0..2]      COMB ; INPUT

;———————— Boolean Equation Segment ———
EQUATIONS
CASE (P[2..0])
        BEGIN
        #b000:                    ;16 BIT PACKING W/ SIGN EXTENSION
                BEGIN
                 Q[3..0] = A[3..0]
                END
        #b001:                    ;8 BIT PACKING
                BEGIN
                 Q[3..0] = B[3..0]
                END
        #b010:                    ;4 BIT PACKING
                BEGIN
                 Q[3..0] = C[3..0]
                END
        #b011:                    ;2 BIT PACKING
                BEGIN
                Q[3..2] = C[1..0]
                Q[1..0] = Q[3..2]
                END
```

```
#b111:                          ;1 BIT PACKING
        BEGIN
         Q[3] = C[0]
        Q[2..0] = Q[3..1]
        END
OTHERWISE:                      ;UNUSED CASES DEFAULT TO O
        BEGIN
         Q[3..0] = 0
        END
END
```

## 8.3 RIPAL02

```
;PALASM Design Description

;———————— Declaration Segment ————————
TITLE       RIPAL02.PDS
PATTERN     TEST PATTERN GENERATOR - SYNC UP COUNTER, ASYN CLR, SYNC
            TOGGLE
REVISION    0
AUTHOR      BILL SISK
COMPANY     ARECIBO OBSERVATORY
DATE        11/10/92

CHIP  RIPAL02  PAL22V10

;———————— PIN Declarations ————————————
PIN  24             VCC
PIN  12             GND
PIN  1              CLK             COMB ; INPUT
PIN  2..9           D[1..8]         COMB ; INPUT
PIN  23..16         Q[1..8]         REG  ; OUTPUT
PIN  15             RCO             COMB ; OUTPUT
PIN  14             ENP             COMB ; INPUT
PIN  10             LD              COMB ; INPUT
PIN  11             CLR             COMB ; INPUT
PIN  13             TOGGLE          COMB ; INPUT
NODE  1             GLOBAL          COMB ; INPUT

;———————— Boolean Equation Segment ————
EQUATIONS
IF /LD * TOGGLE THEN
    BEGIN
    Q[1..8] = D[1..8]
    END
IF LD * TOGGLE * ENP THEN
 BEGIN
  Q[1] = /Q[1]
  Q[2] = Q[2] :+:  Q[1]
  Q[3] = Q[3] :+: (Q[2] * Q[1])
  Q[4] = Q[4] :+: (Q[3] * Q[2] * Q[1])
  Q[5] = Q[5] :+: (Q[4] * Q[3] * Q[2] * Q[1])
  Q[6] = Q[6] :+: (Q[5] * Q[4] * Q[3] * Q[2] * Q[1])
  Q[7] = Q[7] :+: (Q[6] * Q[5] * Q[4] * Q[3] * Q[2] * Q[1])
  Q[8] = Q[8] :+: (Q[7] * Q[6] * Q[5] * Q[4] * Q[3] * Q[2] * Q[1])
END
```

```
IF LD * TOGGLE * /ENP THEN
        BEGIN
        Q[1..8] = Q[1..8]
        END
IF /TOGGLE THEN
        BEGIN
        Q[1..8] = /Q[1..8]
        END
RCO = Q[1] * Q[2] * Q[3] * Q[4] * Q[5] * Q[6] * Q[7] * Q[8]
GLOBAL.RSTF = /CLR
```

**8.4 RIPAL03**

```
;PALASM Design Description

;———————— Declaration Segment ————————
TITLE       RIPAL03.PDS
PATTERN     SYNCHRONOUS 8-BIT BINARY DOWN COUNTER WITH TRI-STATE
            OUTPUTS
REVISION    0
AUTHOR      BILL SISK
COMPANY     ARECIBO OBSERVATORY
DATE        11/5/92

CHIP  RIPAL03  PAL22V10

;———————— PIN Declarations ————————————
PIN  24       VCC
PIN  12       GND
PIN  1        CLK          COMB ; INPUT
PIN  2..9     D[1..8]      COMB ; INPUT
PIN  23..16   Q[1..8]      REG  ; OUTPUT
PIN  15       RCO          COMB ; OUTPUT
PIN  14       OE           COMB ; INPUT
PIN  10       LD           COMB ; INPUT
PIN  11       ENT          COMB ; INPUT
PIN  13       ENP          COMB ; INPUT

;———————— Boolean Equation Segment ———
EQUATIONS
IF LD = 0 THEN
  BEGIN
   Q[1..8] = D[1..8]
  END
ELSE
 BEGIN
  IF ENT * ENP THEN
   BEGIN
    Q[1] = /Q[1]
    Q[2] = Q[2] :+: /Q[1]
    Q[3] = Q[3] :+: (/Q[2] * /Q[1])
    Q[4] = Q[4] :+: (/Q[3] * /Q[2] * /Q[1])
    Q[5] = Q[5] :+: (/Q[4] * /Q[3] * /Q[2] * /Q[1])
    Q[6] = Q[6] :+: (/Q[5] * /Q[4] * /Q[3] * /Q[2] * /Q[1])
    Q[7] = Q[7] :+: (/Q[6] * /Q[5] * /Q[4] * /Q[3] * /Q[2] * /Q[1])
    Q[8] = Q[8] :+: (/Q[7] * /Q[6] * /Q[5] * /Q[4] * /Q[3] * /Q[2] * /Q[1])
   END
```

```
  ELSE
    BEGIN
     Q[1..8] = Q[1..8]
    END
END
RCO = /Q[1] * /Q[2] * /Q[3] * /Q[4] * /Q[5] * /Q[6] * /Q[7] * /Q[8] * ENT
Q[1..8].TRST = /OE
```

## 8.5 RIPAL04.PDS

```
;PALASM Design Description

;————————— Declaration Segment ————————
TITLE        RIPAL04.PDS
PATTERN      SYNCHRONOUS 8-BIT BINARY DOWN COUNTER WITH ASYNC CLEAR
REVISION     0
AUTHOR       BILL SISK
COMPANY      ARECIBO OBSERVATORY
DATE         11/5/92

CHIP  RIPAL04  PAL22V10

; ————————— PIN Declarations ————————————-
PIN  24              VCC
PIN  12              GND
PIN  1               CLK          COMB ; INPUT
PIN  2..9            D[1..8]      COMB ; INPUT
PIN  23..16          Q[1..8]      REG  ; OUTPUT
PIN  15              RCO          COMB ; OUTPUT
PIN  14              CLR          COMB ; INPUT
PIN  10              LD           COMB ; INPUT
PIN  11              ENT          COMB ; INPUT
PIN  13              ENP          COMB ; INPUT
NODE 1               GLOBAL       COMB ; INPUT

;————————— Boolean Equation Segment ———
EQUATIONS
IF LD = 0 THEN
  BEGIN
   Q[1..8] = D[1..8]
  END
ELSE
 BEGIN
  IF ENT * ENP THEN
   BEGIN
    Q[1] = /Q[1]
    Q[2] = Q[2] :+: /Q[1]
    Q[3] = Q[3] :+: (/Q[2] * /Q[1])
    Q[4] = Q[4] :+: (/Q[3] * /Q[2] * /Q[1])
    Q[5] = Q[5] :+: (/Q[4] * /Q[3] * /Q[2] * /Q[1])
    Q[6] = Q[6] :+: (/Q[5] * /Q[4] * /Q[3] * /Q[2] * /Q[1])
    Q[7] = Q[7] :+: (/Q[6] * /Q[5] * /Q[4] * /Q[3] * /Q[2] * /Q[1])
    Q[8] = Q[8] :+: (/Q[7] * /Q[6] * /Q[5] * /Q[4] * /Q[3] * /Q[2] * /Q[1])
   END
```

```
  ELSE
    BEGIN
     Q[1..8] = Q[1..8]
    END
END
RCO = /Q[1] * /Q[2] * /Q[3] * /Q[4] * /Q[5] * /Q[6] * /Q[7] * /Q[8] * ENT
GLOBAL.RSTF = /CLR
```

## 8.6 RIPAL05

```
;PALASM Design Description

;———————— Declaration Segment ————————
TITLE       RIPAL05.PDS
PATTERN     SYNCHRONOUS 8-BIT BINARY UP COUNTER WITH TRI-STATE OUTPUTS
REVISION    0
AUTHOR      BILL SISK
COMPANY     ARECIBO OBSERVATORY
DATE        11/5/92

CHIP  RIPAL05  PAL22V10

;———————— PIN Declarations ————————-
PIN  24              VCC
PIN  12              GND
PIN  1               CLK          COMB ; INPUT
PIN  2..9            D[1..8]      COMB ; INPUT
PIN  23..16          Q[1..8]      REG  ; OUTPUT
PIN  15              RCO          COMB ; OUTPUT
PIN  14              OE           COMB ; INPUT
PIN  10              LD           COMB ; INPUT
PIN  11              ENT          COMB ; INPUT
PIN  13              ENP          COMB ; INPUT

; ———————— Boolean Equation Segment ————
EQUATIONS
IF LD = 0 THEN
      BEGIN
      Q[1..8] = D[1..8]
      END
ELSE
 BEGIN
  IF ENT * ENP THEN
   BEGIN
    Q[1] = /Q[1]
    Q[2] = Q[2] :+:  Q[1]
    Q[3] = Q[3] :+: (Q[2] * Q[1] )
    Q[4] = Q[4] :+: (Q[3] * Q[2] * Q[1] )
    Q[5] = Q[5] :+: (Q[4] * Q[3] * Q[2] * Q[1] )
    Q[6] = Q[6] :+: (Q[5] * Q[4] * Q[3] * Q[2] * Q[1] )
    Q[7] = Q[7] :+: (Q[6] * Q[5] * Q[4] * Q[3] * Q[2] * Q[1] )
    Q[8] = Q[8] :+: (Q[7] * Q[6] * Q[5] * Q[4] * Q[3] * Q[2] * Q[1])
   END
```

```
ELSE
        BEGIN
                Q[1..8] = Q[1..8]
        END
END

RCO = Q[1] * Q[2] * Q[3] * Q[4] * Q[5] * Q[6] * Q[7] * Q[8] * ENT
Q[1..8].TRST = /OE
```

## 8.7 RIPAL06.PDS

```
;PALASM Design Description

;————————— Declaration Segment ————————
TITLE       RIPAL06.PDS
PATTERN     Manchester Code Transmitter
REVISION    0
AUTHOR      BILL SISK
COMPANY     ARECIBO OBSERVATORY
DATE        12/21/92

CHIP  RIPAL06  PAL22V10

;————————————— PIN Declarations ————————————-
PIN  24              VCC
PIN  12              GND
PIN  1               CLK              COMB ; INPUT
PIN  3               CLR              COMB ; INPUT
PIN  2               SERIN            COMB ; INPUT
PIN  14              SRCLK            REG  ; OUTPUT
PIN  23..18          Q[1..6]          REG  ; OUTPUT
PIN  17              XmtReady         REG  ; OUTPUT
PIN  16              SEROUT           REG  ; OUTPUT
PIN  15              SEROUTBAR        COMB ; OUTPUT
NODE 1               GLOBAL           COMB ;

STRING  STOP  '( Q[1] * /Q[2] * /Q[3] * /Q[4] * Q[5] * Q[6] )'  ;Count to 49
;————————— Boolean Equation Segment ————
EQUATIONS
SEROUTBAR = /SEROUT

IF /STOP THEN
        BEGIN
                Q[1] = /Q[1]
                Q[2] = Q[2] :+: Q[1]
                Q[3] = Q[3] :+: ( Q[2] * Q[1] )
                Q[4] = Q[4] :+: ( Q[3] * Q[2] * Q[1] )
                Q[5] = Q[5] :+: ( Q[4] * Q[3] * Q[2] * Q[1] )
                Q[6] = Q[6] :+: ( Q[5] * Q[4] * Q[3] * Q[2] * Q[1] )
                SEROUT =  ( /Q[1] + SERIN ) :+: SEROUT
                SRCLK = Q[1]
                XmtReady = 0
        END
```

```
    ELSE
            BEGIN
                Q[1..6] = Q[1..6]
                SEROUT = 0
                SRCLK = 0
                XmtReady = 1
            END

GLOBAL.RSTF = /CLR
```

## 8.8 RIPAL09

```
;PALASM Design Description

;———————— Declaration Segment ————————
TITLE       RIPAL09.PDS
PATTERN     Sync 4-bit Binary Down Cntr for Input Clk Generator
REVISION    0
AUTHOR      BILL SISK
COMPANY     ARECIBO OBSERVATORY
DATE        11/5/92

CHIP  RIPAL09  PAL22V10

;———————— PIN Declarations ————————————
PIN  24          VCC
PIN  12          GND
PIN  1           CLK          COMB ; INPUT
PIN  2..4        P[0..2]      COMB ; INPUT
PIN  23..20      Q[0..3]      REG  ; OUTPUT
PIN  19          RCO          COMB ; OUTPUT
PIN  18          IN           COMB ; INPUT
PIN  17          GatedOut     COMB ; OUTPUT
PIN  16          EnGate       REG  ; OUTPUT
PIN  5           CLR          COMB ; INPUT
NODE 1           GLOBAL       COM  ; NODE

;———————— Boolean Equation Segment ————
EQUATIONS
IF RCO = 1 THEN                  ; LOAD REGISTERS
        BEGIN
                Q[0] = P[0] + P[1] + P[2]
                Q[1] = P[1]
                Q[2] = P[1] * P[0]
                Q[3] = P[2]
        END
ELSE                             ; COUNT DOWN
        BEGIN
                Q[0] = /Q[0]
                Q[1] = Q[1] :+: /Q[0]
                Q[2] = Q[2] :+: ( /Q[1] * /Q[0] )
                Q[3] = Q[3] :+: ( /Q[2] * /Q[1] * /Q[0] )
        END
```

EnGate = 1

RCO = /Q[0] * /Q[1] * /Q[2] * /Q[3]
GatedOut = RCO * IN * CLR * EnGate

GLOBAL.RSTF = /CLR

## 8.9 RIPAL17.PDS

```
;PALASM Design Description

;————————— Declaration Segment ————————
TITLE       RIPAL17.PDS
PATTERN     TEST PATTERN GENERATOR - SYNC UP COUNTER, ASYN CLR, SYNC
            TOGGLE
REVISION    0
AUTHOR      BILL SISK
COMPANY     ARECIBO OBSERVATORY
DATE        4/16/93

CHIP  RIPAL02  PAL22V10

;————————— PIN Declarations ————————————-
PIN  24             VCC
PIN  12             GND
PIN  1              CLK             COMB ; INPUT
PIN  2..5           D[1..4]         COMB ; INPUT
PIN  23..20         Q[1..4]         REG  ; OUTPUT
PIN  14             ENP             COMB ; INPUT
PIN  10             LD              COMB ; INPUT
PIN  11             CLR             COMB ; INPUT
PIN  13             TOGGLE          COMB ; INPUT
NODE 1              GLOBAL          COMB ; INPUT
PIN  15             IN              COMB ; INPUT
PIN  19             OUT             COMB ; OUTPUT
PIN  18             OUTINV          COMB ; OUTPUT
PIN  6..9           G[1..4]         COMB ; INPUT
PIN  17             AND             COMB ; OUTPUT
PIN  16             NAND            COMB ; OUTPUT

;————————— Boolean Equation Segment ———
EQUATIONS
IF /LD * TOGGLE THEN
    BEGIN
    Q[1..4] = D[1..4]
    END

IF LD * TOGGLE * ENP THEN
      BEGIN
            Q[1] = /Q[1]
            Q[2] = Q[2] :+:  Q[1]
            Q[3] = Q[3] :+: ( Q[2] * Q[1] )
            Q[4] = Q[4] :+: ( Q[3] * Q[2] * Q[1] )
       END
```

```
IF LD * TOGGLE * /ENP THEN
        BEGIN
          Q[1..4] = Q[1..4]
        END

IF /TOGGLE THEN
        BEGIN
          Q[1..4] = /Q[1..4]
        END

GLOBAL.RSTF = /CLR
OUT = IN
OUTINV = /IN
AND = G[1] * G[2] * G[3] * G[4]
NAND = /(G[1] * G[2] * G[3] * G[4])
```

## 8.10 RIPAL18

```
;PALASM Design Description

;———————— Declaration Segment ————————
TITLE       RIPAL18.PDS
PATTERN     SYNC 8-BIT DOWN COUNTER w/ TRI-STATE OUTPUTS,
            (modified RCO)
REVISION    0
AUTHOR      BILL SISK
COMPANY     ARECIBO OBSERVATORY
DATE        11/5/92

CHIP  RIPAL18  PAL22V10

;————————— PIN Declarations ————————————
PIN  24          VCC
PIN  12          GND
PIN  1           CLK          COMB ; INPUT
PIN  2..9        D[1..8]      COMB ; INPUT
PIN  23..16      Q[1..8]      REG  ; OUTPUT
PIN  15          RCO          COMB ; OUTPUT
PIN  14          OE           COMB ; INPUT
PIN  10          LD           COMB ; INPUT
PIN  11          ENT          COMB ; INPUT
PIN  13          ENP          COMB ; INPUT

;———————— Boolean Equation Segment ———
EQUATIONS
IF LD = 0 THEN
  BEGIN
   Q[1..8] = D[1..8]
  END
ELSE
 BEGIN
  IF ENT * ENP THEN
   BEGIN
    Q[1] = /Q[1]
    Q[2] = Q[2] :+: /Q[1]
    Q[3] = Q[3] :+: (/Q[2] * /Q[1] )
    Q[4] = Q[4] :+: (/Q[3] * /Q[2] * /Q[1] )
    Q[5] = Q[5] :+: (/Q[4] * /Q[3] * /Q[2] * /Q[1] )
    Q[6] = Q[6] :+: (/Q[5] * /Q[4] * /Q[3] * /Q[2] * /Q[1] )
    Q[7] = Q[7] :+: (/Q[6] * /Q[5] * /Q[4] * /Q[3] * /Q[2] * /Q[1])
    Q[8] = Q[8] :+: (/Q[7] * /Q[6] * /Q[5] * /Q[4] * /Q[3] * /Q[2] * /Q[1])
   END
```

```
ELSE
   BEGIN
    Q[1..8] = Q[1..8]
   END
END
RCO = /Q[1] * /Q[2]* /Q[3] * /Q[4] * /Q[5] * /Q[6] * /Q[7] * /Q[8] * ENT * ENP
Q[1..8].TRST = /OE
```

## 8.11 RIPAL30

```
;PALASM Design Description

;———————— Declaration Segment ————————
TITLE       RIPAL30.PDS
PATTERN     VME RADAR INTERFACE
REVISION    0
AUTHOR      BILL SISK
COMPANY     ARECIBO OBSERVATORY
DATE        8/10/93

CHIP  RIPAL30  PAL29MA16

;———————— PIN Declarations ————————————-
PIN  24                 VCC
PIN  12                 GND
PIN  22..15             UD[7..0]        COMB; OUTPUT
PIN  10..5              UA[7..2]        COMB; OUTPUT
PIN  4                  UVIC            COMB; OUTPUT
PIN  2                  MvInit          COMB; INPUT
PIN  13                 MvExit          COMB; INPUT
PIN  14                 Inter           COMB; INPUT
PIN  23                 RegIn           COMB; INPUT
PIN  11                 UBG             COMB; INPUT

;———————— Boolean Equation Segment ————
EQUATIONS

IF MvInit * /MvExit * /Inter THEN
        BEGIN
                UD[7..0] = #H20
        END
IF /MvInit * MvExit * /Inter THEN
        BEGIN
                UD[7..0] = #H00
        END
IF /MvInit * /MvExit * Inter THEN
        BEGIN
                UD[7..0] = #H11
        END
IF (MvInit + MvExit) * /Inter THEN
        BEGIN
                UA[7..2] = #B110101 ;UA[7..0] = #HD4
        END
```

```
IF /(MvInit + MvExit) * Inter THEN
        BEGIN
                UA[7..2] = #B100000;UA[7..0] = #H80
        END

/UVIC = RegIn * /UBG
UD[7..0].TRST = RegIn * /UBG
UA[7..2].TRST = RegIn * /UBG
```

8.12 RIPAL31

```
;PALASM Design Description

;---------- Declaration Segment ----------
TITLE   RIPAL31.PDS
PATTERN  VME RADAR INTERFACE, VP1 BOARD STATE MACHINE
REVISION 1
AUTHOR   BILL SISK
COMPANY  ARECIBO OBSERVATORY
DATE    4/7/97

CHIP  RIPAL31  PAL22V10

;---------- PIN Declarations ----------
PIN  24        VCC
PIN  12        GND
PIN  1         CLK          COMB ; INPUT
PIN  2         Movem        COMB ; INPUT
PIN  3         WordX        COMB ; INPUT
PIN  4         WCC          COMB ; INPUT
PIN  5         BoundaryX    COMB ; INPUT
PIN  6         FifoEmp      COMB ; INPUT
PIN  7         FFLtch       COMB ; INPUT
PIN  8         VBR          COMB ; INPUT
PIN  9         CLR          COMB ; INPUT
PIN  10        UBG          COMB ; INPUT
PIN  11        DelUBG       COMB ; INPUT
PIN  13        FELtch       COMB ; INPUT
PIN  23        UBR          COMB  ; OUTPUT
PIN  22        MvInit       COMB  ; OUTPUT
PIN  21        MvExit       COMB  ; OUTPUT
PIN  20        Inter        COMB  ; OUTPUT
PIN  19        Master       COMB  ; OUTPUT
PIN  18        BIT0         REG ;
PIN  17        BIT1         REG ;
PIN  16        BIT2         REG ;
PIN  15        CycleClk     COMB ; OUTPUT
```

```
;---------------- State Segment ----------------
STATE
MOORE_MACHINE

START_UP := POWER_UP -> Null
CLKF = CLK  ;  CLK is /UDSACK0*

Null            :=  MovemGo -> MovemEnter
                +   WordxGo -> DataXfer
                +-> Null

MovemEnter  :=  MovemGo -> DataXfer
                +-> MovemExit

DataXfer        := MovemPark -> DataXfer
                + MvRestart -> MovemExit
                + MovemStop -> MovemExit
                + WordxGo   -> DataXfer
                + WordxStop -> WrtInter
                +-> Null

MovemExit   := MovemStop -> WrtInter
                + MovemGo -> MovemEnter
                +-> Null

WrtInter        := MovemStop -> Null
        + WordxStop -> Null
        +-> Null

Null =          /BIT2 * /BIT1 * /BIT0
DataXfer =      /BIT2 * /BIT1 *  BIT0
MovemEnter = BIT2 * /BIT1 *  BIT0
MovemExit =   BIT2 * /BIT1 * /BIT0
WrtInter =      BIT2 *  BIT1 * /BIT0

Null.OUTF       = /MvInit * /Master * /MvExit * /Inter
MovemEnter.OUTF =  MvInit * /Master * /MvExit * /Inter
DataXfer.OUTF   = /MvInit *  Master * /MvExit * /Inter
MovemExit.OUTF  = /MvInit * /Master *  MvExit * /Inter
WrtInter.OUTF   =  /MvInit * /Master * /MvExit *  Inter
```

```
CONDITIONS
MovemGo    = Movem * /WordX * /(WCC + FifoEmp * FFLtch)
MvRestart  = Movem * /WordX * /(WCC + FifoEmp * FFLtch) * (BoundaryX + FELtch)
MovemPark  = Movem * /WordX * /(WCC + FifoEmp * FFLtch) * /(BoundaryX + FELtch)
MovemStop  = Movem * /WordX *  (WCC + FifoEmp * FFLtch)
WordxGo    =/Movem *  WordX * /(WCC + FifoEmp * FFLtch)
WordxStop  =/Movem *  WordX *  (WCC + FifoEmp * FFLtch)

;---------- Boolean Equation Segment --------
EQUATIONS
/UBR =  CLR * (VBR * /BIT2 * /BIT1 * BIT0 + BIT2)
CycleClk = MASTER * /UBG * VBR * /FifoEmp * /CLK  +
                BIT2 * /UBG * /DelUBG * /CLK
```

## 8.12 RIPAL31

```
;PALASM Design Description

;————————— Declaration Segment ————————
TITLE       RIPAL31.PDS
PATTERN     VME RADAR INTERFACE, VP1 BOARD STATE MACHINE
REVISION    0
AUTHOR      BILL SISK
COMPANY     ARECIBO OBSERVATORY
DATE        8/11/93

CHIP RIPAL31 PAL22V10

;————————— PIN Declarations ————————————
PIN 24          VCC
PIN 12          GND
PIN 1           CLK         COMB ; INPUT
PIN 2           Movem       COMB ; INPUT
PIN 3           WordX       COMB ; INPUT
PIN 4           WCC         COMB ; INPUT
PIN 5           BoundaryX   COMB ; INPUT
PIN 6           FifoEmp     COMB ; INPUT
PIN 7           FFLtch      COMB ; INPUT
PIN 8           VBR         COMB ; INPUT
PIN 9           CLR         COMB ; INPUT
PIN 10          UBG         COMB ; INPUT
PIN 11          DelUBG      COMB ; INPUT
PIN 23          UBR         COMB ; OUTPUT
PIN 22          MvInit      COMB ; OUTPUT
PIN 21          MvExit      COMB ; OUTPUT
PIN 20          Inter       COMB ; OUTPUT
PIN 19          Master      COMB ; OUTPUT
PIN 18          BIT0        REG  ;
PIN 17          BIT1        REG  ;
PIN 16          BIT2        REG  ;
PIN 15          CycleClk    COMB ; OUTPUT
```

```
;————————— State Segment ————————————————
STATE
MOORE_MACHINE

START_UP := POWER_UP -> Null
CLKF = CLK  ;  CLK is /UDSACK0*

Null          := MovemGo -> MovemEnter
              +  WordxGo -> DataXfer
              +-> Null

MovemEnter    := MovemGo -> DataXfer
              +-> MovemExit

DataXfer      := MovemPark -> DataXfer
              + MvRestart -> MovemExit
              + MovemStop -> MovemExit
              + WordxGo  -> DataXfer
              + WordxStop -> WrtInter
              +-> Null

MovemExit     := MovemStop -> WrtInter
              + MovemGo -> MovemEnter
              +-> Null

WrtInter      := MovemStop -> Null
              + WordxStop -> Null
              +-> Null

Null                    =/BIT2 * /BIT1 * /BIT0
DataXfer                =/BIT2 * /BIT1 *  BIT0
MovemEnter              = BIT2 * /BIT1 * /BIT0
MovemExit               = BIT2 * /BIT1 *  BIT0
WrtInter                = BIT2 *  BIT1 * /BIT0

Null.OUTF               = /MvInit * /Master * /MvExit * /Inter
MovemEnter.OUTF         =  MvInit * /Master * /MvExit * /Inter
DataXfer.OUTF           = /MvInit *  Master * /MvExit * /Inter
MovemExit.OUTF          = /MvInit * /Master *  MvExit * /Inter
WrtInter.OUTF           = /MvInit * /Master * /MvExit *  Inter
```

```
CONDITIONS
MovemGo      = Movem * /WordX * /(WCC + FifoEmp * FFLtch)
MvRestart    = Movem * /WordX * /(WCC + FifoEmp * FFLtch) * (BoundaryX + FifoEmp)
MovemPark    = Movem * /WordX * /(WCC + FifoEmp * FFLtch) */(BoundaryX + FifoEmp)
MovemStop    = Movem * /WordX *  (WCC + FifoEmp * FFLtch)
WordxGo      =/Movem *  WordX * /(WCC + FifoEmp * FFLtch)
WordxStop    =/Movem *  WordX *  (WCC + FifoEmp * FFLtch)

;————————— Boolean Equation Segment ———
EQUATIONS

/UBR =  CLR * ( VBR * Master + BIT2 )
CycleClk = Master * /UBG * VBR * /FifoEmp * /CLK  +  BIT2 * /UBG * /DelUBG * /CLK
```

## 8.13 RIPAL32

```
;PALASM Design Description

;————————— Declaration Segment ————————
TITLE       RIPAL32.PDS
PATTERN     VME RADAR INTERFACE
REVISION    0
AUTHOR      BILL SISK
COMPANY     ARECIBO OBSERVATORY
DATE        8/11/93

CHIP RIPAL32 PAL20RA10

;————————— PIN Declarations ————————————-
PIN 24          VCC
PIN 12          GND
PIN 1           PL          COMB ; INPUT
PIN 13          OE          COMB ; INPUT
PIN 2           EFCH1       COMB ; INPUT
PIN 3           EFCH2       COMB ; INPUT
PIN 4           FFCH1       COMB ; INPUT
PIN 5           FFCH2       COMB ; INPUT
PIN 6           HFCH1       COMB ; INPUT
PIN 7           HFCH2       COMB ; INPUT
PIN 8           SelCh1      COMB ; INPUT
PIN 9           CLR         COMB ; INPUT
PIN 10          FifoClk     COMB ; INPUT
PIN 11          SoftFifoWrt COMB ; INPUT
PIN 14          TestMode    COMB ; INPUT
PIN 23          EF          COMB ; OUTPUT
PIN 22          FF          COMB ; OUTPUT
PIN 21          HF          COMB ; OUTPUT
PIN 20          FFLtch      REG
PIN 19          FCLK        COMB ; OUTPUT
```

```
;————————— Boolean Equation Segment ———
EQUATIONS
; Note!  The 20RA10 .SETF and .RSTF are control Q of the register.
; The output is reversed is polarity.  Thus, the normal .SETF and
; .RSTF below are reversed.

EF = /SelCh1 * /EFCH1 +  SelCh1 * /EFCH2
FF = /SelCH1 * /FFCH1 +  SelCH1 * /FFCH2
HF = /SelCH1 * /HFCH1 +  SelCH1 * /HFCH2

FFLtch.RSTF = FF
FFLtch.SETF = /CLR
FFLtch.CLKF = VCC
FFLtch = VCC

FCLK = FifoClk * TestMode + SoftFifoWrt * /TestMode
```

## 8.14 RIPAL33

```
;PALASM Design Description

;———————— Declaration Segment ————————
TITLE       RIPAL33.PDS
PATTERN     VME RADAR INTERFACE
REVISION    0
AUTHOR      BILL SISK
COMPANY     ARECIBO OBSERVATORY
DATE        8/11/93

CHIP RIPAL33 PAL20RA10

;———————— PIN Declarations ————————
PIN 24          VCC
PIN 12          GND
PIN 1           PL          COMB ; INPUT
PIN 13          OE          COMB ; INPUT
PIN 2           UDSACK      COMB ; INPUT
PIN 3           Master      COMB ; INPUT
PIN 4           UBG         COMB ; INPUT
PIN 5           Cycle       COMB ; INPUT
PIN 6           Delay       COMB ; INPUT
PIN 7           DelayX      COMB ; INPUT
PIN 8           PrCh1       COMB ; INPUT
PIN 9           SelCh2      COMB ; INPUT
PIN 10          WrtAdr      COMB ; INPUT
PIN 11          WrtWC       COMB ; INPUT
PIN 23          UAS         REG
PIN 22          UDS         REG
PIN 21          RdCH1       COMB ; OUTPUT
PIN 20          RdCH2       COMB ; OUTPUT
PIN 19          RdLatch     COMB ; OUTPUT
PIN 18          AdrClk      COMB ; OUTPUT
PIN 17          WCClk       COMB ; OUTPUT
PIN 16          QMas        REG
PIN 15          CH1         REG
```

```
;————————— Boolean Equation Segment ———
EQUATIONS

; Note!  The 20RA10 .SETF and .RSTF are control Q of the register.
; The output is reversed is polarity.  Thus, the normal .SETF and
; .RSTF below are reversed.

QMas = Master
QMas.CLKF = UDSACK
AdrClk = QMas * /UBG * /UDSACK + /WrtAdr
WCClk = Master * (Cycle * /Delay) + /WrtWC

CH1.SETF = /SelCh2          ;CH2 selected
CH1.RSTF = /PrCh1           ;CH1 selected, CH1 = Active High
CH1 = /CH1
CH1.CLKF = QMas * /UBG * /UDSACK

/RdCh1 =  CH1 * Master * (Cycle * /Delay)
/RdCh2 = /CH1 * Master * (Cycle * /Delay)
RdLatch = Master * (Cycle * /Delay)

/UAS = VCC
/UDS = VCC
UAS.CLKF = Delay
UDS.CLKF = Delay
UAS.RSTF = /UDSACK
UDS.RSTF = /UDSACK
UAS.TRST = /UBG
UDS.TRST = /UBG
```

## 8.15 RIPAL35

```
;PALASM Design Description

;———————— Declaration Segment ————————
TITLE       RIPAL35.PDS
PATTERN     RI VP1 BOARD COMMAND WORD DECODER & LATCH
REVISION    0
AUTHOR      BILL SISK
COMPANY     ARECIBO OBSERVATORY
DATE        8/12/93

CHIP  RIPAL35  PAL29MA16

;———————— PIN Declarations ————————————
PIN  24              VCC
PIN  12              GND
PIN  1               CLK              COMB ; INPUT
PIN  13..19          UD[0..6]         COMB ; INPUT
PIN  2               AltAck           COMB ; INPUT
PIN  11              ACK              COMB ; INPUT
PIN  23              RES              COMB ; INPUT
PIN  22              Inter            COMB ; INPUT
PIN  10              ClrMas           COMB ; OUTPUT
PIN  21              ClrReset         COMB ; OUTPUT
PIN  20              CLR              REG
PIN  4               WORDX            REG
PIN  5               MOVEM            REG
PIN  6               SelCh1           REG
PIN  7               SelCh2           REG
PIN  8               PrCh1            COMB ; OUTPUT
PIN  9               TESTMODE         REG
PIN  3               UNUSED           COMB

;———————————— Boolean Equation Segment ————
EQUATIONS

CASE (UD[0])
        BEGIN
        #b0:
                BEGIN
                CLR = CLR
                END
        #b1:
                BEGIN
                CLR = 0
                END
        END
```

```
ClrReset = /AltAck * /TESTMODE + /ACK * TESTMODE
CLR.SETF = ClrReset

CASE (UD[2..1])
        BEGIN
        #b00:
                BEGIN
                        WORDX = WORDX           ; NOP
                        MOVEM = MOVEM
                END
        #b01:
                BEGIN
                        WORDX = 1               ; enable single word
                        MOVEM = 0               ; data transfer
                END
        #b10:
                BEGIN
                        WORDX = 0               ; enable Movem data
                        MOVEM = 1               ; transfer
                END
        #b11:
                BEGIN
                        WORDX = 0               ; disable data transfer
                        MOVEM = 0
                END
        END

ClrMas = /RES + Inter
MOVEM.RSTF = ClrMas                             ; data transfer disabled on startup
WORDX.RSTF = ClrMas

CASE (UD[4..3])                                 ; Selected channel is active low
        BEGIN
        #b00:
                BEGIN
                        SelCh1 = SelCh1         ; NOP
                        SelCh2 = SelCh2
                END
        #b01:
                BEGIN
                        SelCh1 = 0              ; enable CH1
                        SelCh2 = 1              ; disable CH2
                END
```

```
        #b10:
                BEGIN
                        SelCh1 = 1              ; disable CH1
                        SelCh2 = 0              ; enable CH2
                END
        #b11:
                BEGIN
                        SelCh1 = 1              ; enable Alt CH
                        SelCh2 = 1
                END
        END

SelCh1.RSTF = /RES                              ; CH1 enabled on startup
SelCh2.SETF = /RES                              ; CH2 disabled on startup
/PrCh1 = /SelCh1 + SelCh1 * SelCh2 * /CLR

CASE (UD[6..5])                                 ; testmode - active low
        BEGIN
        #b00:
                BEGIN
                        TESTMODE = TESTMODE ; NOP
                END
        #b01:
                BEGIN
                        TESTMODE = 1            ; disable testmode
                END
        #b10:
                BEGIN
                        TESTMODE = 0            ; enable testmode
                END
        #b11:
                BEGIN
                        TESTMODE = TESTMODE ; NOP
                END
        END

TESTMODE.SETF = /RES                            ; testmode disabled on startup

/CLR.CLKF = CLK
/MOVEM.CLKF = CLK
/WORDX.CLKF = CLK
/SelCh1.CLKF = CLK
/SelCh2.CLKF = CLK
/TESTMODE.CLKF = CLK

UNUSED = GND
```

## 8.16 RIPAL36

```
;PALASM Design Description

;————————————— Declaration Segment ————————————
TITLE        RIPAL36.PDS
PATTERN      RI FIFO BOARD ADDRESS DECODER
REVISION     0
AUTHOR       BILL SISK
COMPANY      ARECIBO OBSERVATORY
DATE         8/16/93

CHIP RIPAL36 PAL20RA10

;-————————————— PIN Declarations ——————————————-
PIN 24              VCC
PIN 12              GND
PIN 1               PL              COMB ; INPUT
PIN 13              OE              COMB ; INPUT
PIN 2               UA2             COMB ; INPUT
PIN 3               UA3             COMB ; INPUT
PIN 4               UD7             COMB ; INPUT
PIN 5               IPP             COMB ; INPUT
PIN 6               DelaySlv        COMB ; INPUT
PIN 7               URW             COMB ; INPUT
PIN 8               FC1             COMB ; INPUT
PIN 9               UDS             COMB ; INPUT
PIN 11              VBG             COMB ; INPUT
PIN 23              IPPReg          REG
PIN 22              /ACK0           REG
PIN 21              /ACK1           REG
PIN 20              /WrtAdr         COMB; OUTPUT
PIN 19              /WrtWC          COMB; OUTPUT
PIN 18              /ComWd          COMB; OUTPUT
PIN 17              SoftFifoWrt     COMB; OUTPUT
PIN 16              /RdStatus       COMB; OUTPUT
PIN 15              Slave           COMB; OUTPUT
PIN 14              /AltAck         REG
```

```
;————————— Boolean Equation Segment ———
EQUATIONS

WrtAdr =          /UA3 * /UA2 * /URW * /FC1 * /VBG * /UDS
WrtWC =           /UA3 *  UA2 * /URW * /FC1 * /VBG * /UDS
ComWd =            UA3 * /UA2 * /URW * /FC1 * /VBG * /UDS
SoftFifoWrt =      UA3 *  UA2 * /URW * /FC1 * /VBG * /UDS
RdStatus =         URW * /FC1 * /VBG * /UDS
Slave =           /FC1 * /VBG * /UDS

; Slave Acknowlegde - UDSACK0* & UDSACK1*
ACK0 = VCC
ACK1 = VCC
AltAck = VCC

ACK0.CLKF = DelaySlv
ACK1.CLKF = DelaySlv
AltAck.CLKF = DelaySlv

ACK0.RSTF =  /Slave
ACK1.RSTF =  /Slave
AltAck.RSTF = /Slave

ACK0.TRST = /VBG
ACK1.TRST = /VBG

; IPP Register

IPPReg = VCC
IPPReg.CLKF = IPP
IPPReg.SETF = ComWd * UD7
```

## 8.17 RIPAL37

```
;PALASM Design Description

;———————— Declaration Segment ————————
TITLE       RIPAL37.PDS
PATTERN     SYNCHRONOUS 6-BIT BINARY UP COUNTER WITH TRI-STATE OUTPUTS
REVISION    0
AUTHOR      BILL SISK
COMPANY     ARECIBO OBSERVATORY
DATE        8/20/93

CHIP  RIPAL37  PAL22V10

;———————— PIN Declarations ————————————
PIN  24          VCC
PIN  12          GND
PIN  1           CLK          COMB ; INPUT
PIN  2..7        D[1..6]      COMB ; INPUT
PIN  23..18      Q[1..6]      REG  ; OUTPUT
PIN  17,16       A[1..0]      COMB ; OUTPUT
PIN  15          RCO          COMB ; OUTPUT
PIN  8           LD           COMB ; INPUT
PIN  11          Master       COMB ; INPUT
PIN  13          UBG          COMB ; INPUT
PIN  14          MasBG        COMB ; OUTPUT

; ———————— Boolean Equation Segment ————
EQUATIONS
IF LD = 0 THEN
     BEGIN
     Q[1..6] = D[1..6]
     END
ELSE
       BEGIN
     Q[1] = /Q[1]
     Q[2] = Q[2] :+:  Q[1]
     Q[3] = Q[3] :+: ( Q[2] * Q[1] )
     Q[4] = Q[4] :+: ( Q[3] * Q[2] * Q[1] )
     Q[5] = Q[5] :+: ( Q[4] * Q[3] * Q[2] * Q[1] )
     Q[6] = Q[6] :+: ( Q[5] * Q[4] * Q[3] * Q[2] * Q[1] )
       END

RCO = Q[1] * Q[2] * Q[3] * Q[4] * Q[5] * Q[6]
Q[1..6].TRST = Master * /UBG
A[1..0] = GND
A[1..0].TRST = /UBG
/MasBG = Master * /UBG
```