File : LONG_PNCODE.DOC
Date : 9/17/98
Subject : 40-bit PN Code Generator - Software Requirements

Table 1. IOSelA Address Decoder (A6..A1)

Addr Hex	R/W*	Data	Command
00	0	D[15..0]	Load Code Start Bits 15..0 (+)
01	0	D[15..0]	Load Code Start Bits 31..16 (+)
02	0	D[15..0]	Load Code Start Bits 39..32 (+)
03	0	D[11..0]	Load Shift Enable Length (N-1) (+)
04	0	D[1..0]	Write Command Word (Table 2)
05	0	D[1..0]	Load Configuration Bits (Table 3)
00	1	D[15..0]	Read Code Shift Register 15..0 (+)
01	1	D[15..0]	Read Code Shift Register 31..16 (+)
02	1	D[15..0]	Read Code Shift Register 39..32 (+)
03	1	D[11..0]	Read Shift Enable Length
04	1	D[2..0]	Read Status (Table 4)

(+) Shift Enable must be stopped.
Note 1: The shift enable length (baud length) is 12 Bits.
Note 2: The code start bits can be read back by reading the code shift register before Shift Enable has been started.

Table 2. Command Word

Bits	Command
1,0	Shift Enable Start Mode 0 : Stop 1 : Stop synchronously with external clock. 2 : Start on trigger. 3 : Start immediate.

Table 3. Configuration Word

Bits	Command
0	Clock Selection 0 : Clock is a rear panel 20MHz sinewave input. 1 : Clock is a front panel TTL input.
1	S-Band Code Selection 0 : Code is from memory code generator. 1 : Code is 40-bit pncode generator.

Table 4. Status Word

Bit	Description
0	Shift Enable is enabled (Trigger has occurred.)
1	Clock is front panel TTL input.
2	S-Band Code is from 40-bit pncode generator.