

EALFA / PALFA BASEBAND MIXERS

Theory of operation & Circuit Description

Introduction:

The purpose of this subsystem is to convert a 300-MHz segment of IF spectrum originating in the ALFA receivers to quadrature baseband signals for subsequent A/D conversion. The design is targeted at an input spectrum spanning 100 to 400 MHz. However, the maximum sample rate of the A/D converters is only about 200 MHz, so it is necessary to split the input band into two sub-bands, each 150 MHz wide, so that the highest frequency component in any of the outputs is comfortably less than 100 MHz (75 MHz in reality). The nominal LO frequencies for this subsystem are 175 MHz for the “IF low band” and 325 MHz for the “IF high band”.

Note that there is some potential for confusion about “low band” versus “high band”. The IF low and high bands are reversed from the RF or “sky” low and high bands because the ALFA system’s 1st LO frequency is higher than the top of the RF band, resulting in a frequency order inversion. In this document the terms “low band” and “high band” will always refer to the IF frequency domain unless otherwise noted.

Note that the ALFA system includes a total of fourteen receiver channels to accommodate two polarizations for each of seven “pixels”. This baseband mixer system will also comprise fourteen channels, partitioned as one channel per board. The two boards for a pixel’s two polarizations will be mounted in a common 1RU box. Seven pixels, seven boxes. Each box will provide two well-isolated sets of outputs, comprising 16 individual signals, derived from two sets * two sub-bands * two polarizations * two “phases” (I & Q).

This discussion will cover only a single channel, which does include both sub-bands. And the discussion will concentrate on only one sub-band, because the other sub-band is virtually identical except for filter passband limits and a different model number for the quadrature hybrid used as the LO splitter.

Notes regarding the figures:

For the following please refer to Figure 1 (block diagram) and Figures 2 through 17 (ORCAD diagrams). For most of the discussion you will be able to follow along using either Figure 1 or Figure 2, and references to other figures will mostly be optional pointers to more detailed schematics for the curious. In some cases, however, references to the underlying schematics will be important; the relevant figures will be emphatically pointed out in such cases. The reference designators used in the block diagram correspond to those used in the actual ORCAD schematics. The block diagram also includes information about anticipated maximum signal levels.

The component references made in the course of the discussion will generally be limited to those for the low band path (and for the EALFA 'I' channel sub-paths beyond the demodulator stage), and schematics are only provided within the same constraint. With the exception of the different quadrature hybrid in the high band demodulator block, the schematics for the corresponding blocks in other paths are identical except for different reference designators.

Signal Flow Description:

The full bandwidth input signal is applied to J3, whereupon it is split into two identical signals by H1-1 (Figure 3). One of these signals is destined to be filtered for the low sub-band (100-250 MHz, hereafter referred to simply as the low band), and the other is filtered for the high band (250-400 MHz). Note that in the present design only lowpass filters are used, for two reasons: flexibility and economy. It was thought that some users could benefit from the ability to slightly modify the choice of IF frequencies, and using full bandpass filtering would restrict this freedom. The ECB design does, however, include pads for the inclusion of appropriate highpass filters in one or both paths as well, in the event that unforeseen problems arise from the exclusive use of lowpass filters.

Now let's pursue the signal through the low band. Following the low band filter (LPF1), the signal passes through a programmable step attenuator (H2-1, Figure 4) which gives 1 dB granularity over an attenuation range of about 30 db.

Note that the matter of what signal levels to push through this system is fraught with compromise. A high signal level reduces the relative contribution of noise, ingress, and A/D spurs, at the price of reduced dynamic range. That is, the system will be more susceptible to development of intermodulation products and will be driven deeper into saturation by the high-amplitude radar pulses that inhabit portions of the L-band. Operating with a low signal level, on the other hand, leaves the user with increased corruption from the inevitable essentially fixed-amplitude disturbances such as A/D spurs, ingress of various signals due to imperfect shielding, etc. The purpose for providing user control of the step attenuator settings is to allow the user to select the best compromise for his/her particular application. It is anticipated that with experience, a reasonably-fixed set of good attenuator settings for each general observing application will emerge.

Next the signal passes through two gain stages (H3-1 & H3-3, Figures 5 & 6) with an intermediate fixed attenuator (U5). Unfortunately the input signal frequently includes the high-amplitude radar pulses alluded to earlier, and the intermediate attenuators seen at several places in this design are chosen to avoid the risk of outright burnout of subsequent stages. It may be instructive to review the signal level captions on Figure 1. This architecture of alternating gain and attenuation stages also provides the benefits of better reverse isolation through the path as well as avoiding the risk of instabilities or oscillation if some of the amplifiers are not as unconditionally stable as the manufacturer claims.

Following the second gain stage, the low band signal is once again split into two paths, by H1-2 (Figure 3). The primary path takes the signal through attenuator U4 to the quadrature mixer block H4-1 (now definitely check out Figure 8). We'll get back to the secondary path later.

Within the mixer block the signal is split yet another time by H1, to the two diode ring mixers U40 & U45. These mixers are also provided LO signals which are in quadrature phase, having been passed through amplifier U43 and the quadrature hybrid U42. The two LO signals also pass through attenuators U41 & U44 on their way to the mixers in order to provide better terminations to the outputs of U42 in order to obtain the best possible quadrature phase accuracy (we hope!).

The in-phase (I) and quadrature-phase (Q) mixer outputs each pass through an attenuator (U3 for 'I', U12 for 'Q') to provide good broadband terminations to the mixers' IF ports, then to 75 MHz lowpass filters LPF2 and LPF3. It is these filters that are primarily responsible for blocking undesired high frequency energy that would cause aliasing in the A/D converters, which will normally be operated at a sample rate of 170 MHz. Note that the I & Q signals need flat response down to nearly zero frequency for the remainder of the signal path to the A/D converters- this factor will impact the design of subsequent stages.

Next, the band-limited I & Q signals are each split into two paths for the two isolated outputs, using resistive splitters for the sake of their DC frequency response. Resistive splitters, however, provide very poor isolation between their outputs; therefore the remainder of the path includes multiple amplifiers (H5-1 & H6-1) along with attenuators U1 & U2 in order to provide good reverse isolation. In the event that one output of each pair is left unterminated, negligible impact occurs to the other output.

Note that the amplifiers H5-1 & H6-1 (Figures 9 & 10, respectively) deviate from standard practice in that the inductors usually found in the bias networks are omitted, making it practical to obtain reasonably flat frequency response down to very low frequencies. The price paid is slightly reduced values for the gain and for the maximum output level from the amplifiers.

Now let's carry on with the previously-deferred discussion of the secondary signal path following the splitter H1-2. The purpose of this path is to provide an analog square-law-detected output for convenience in setting the step attenuator and for quick verification that reasonable signal levels are present. The signal passes through attenuator U8, amplifier H3-5 (Figure 5), and attenuator U9 on its way to the detector module H7-1 (now see Figure 11). The detector module includes a simple diode detector (R44, D1, & C49) followed by gain stage U47A and inverter stage U47B. This detector is operated in the square law regime for reasonable system noise levels, but will generally be pushed beyond the square law regime by the radar pulses. Together, these stages provide a very low DC drift differential output with a nominal sensitivity of 100 mV / μ W (based on datasheet specifications for the detector diode).

The detector's differential output is brought to pin jacks on the front panel; additionally the detector's output may read back via the attenuator control interface (H8, please see Figure 12).

The high-band signal path is identical to that of the low-band, with two exceptions:

- The lowpass filter cutoff is nominally 400 MHz instead of 250 MHz.
- The LO frequency is nominally 325 MHz instead of 175 MHz.
- The quadrature hybrid used in the demodulator block is a different model for the higher LO frequency.

EALFA/PALFA BASEBAND MIXER

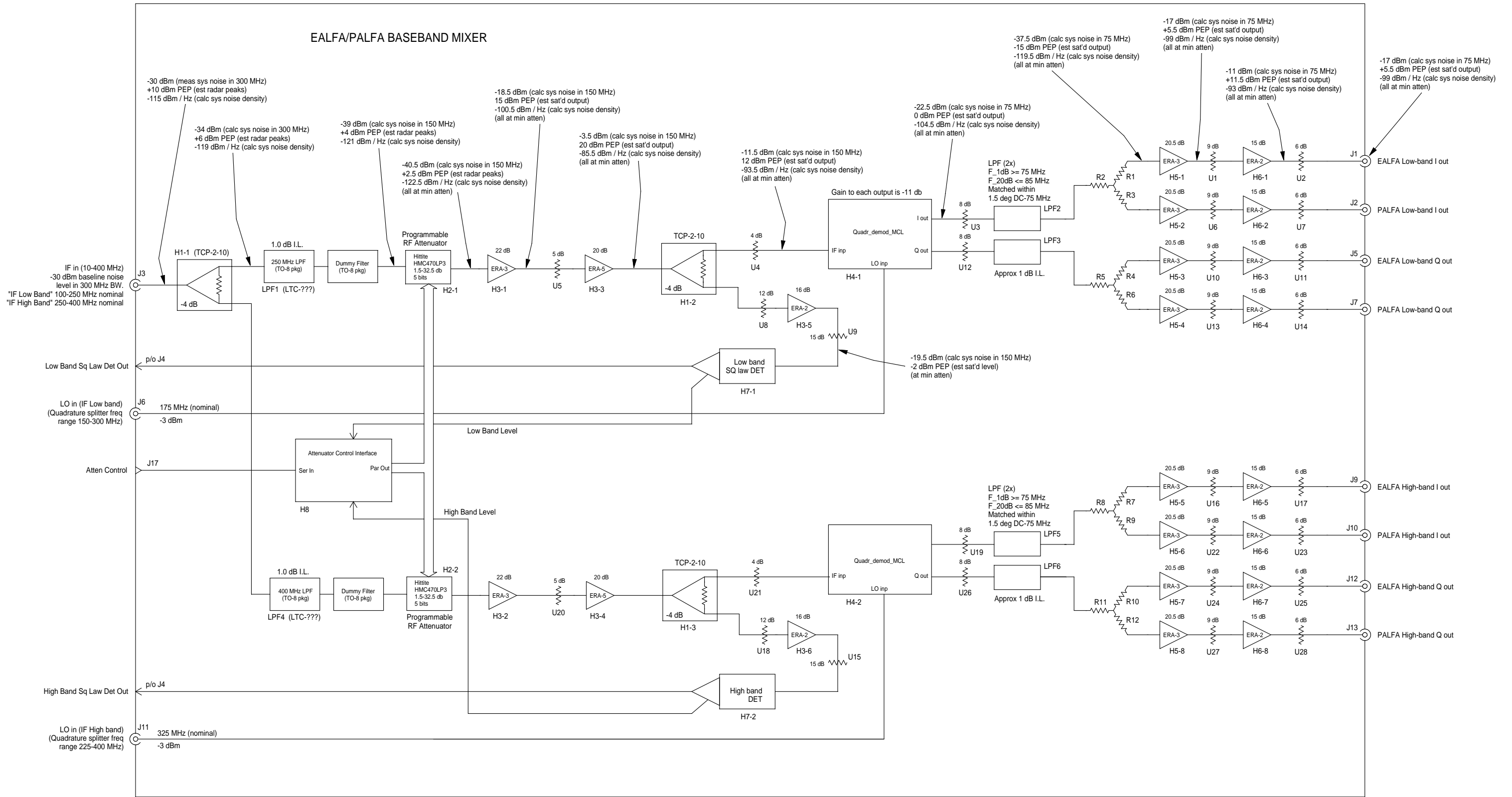
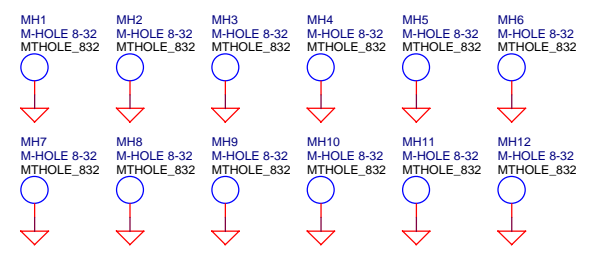
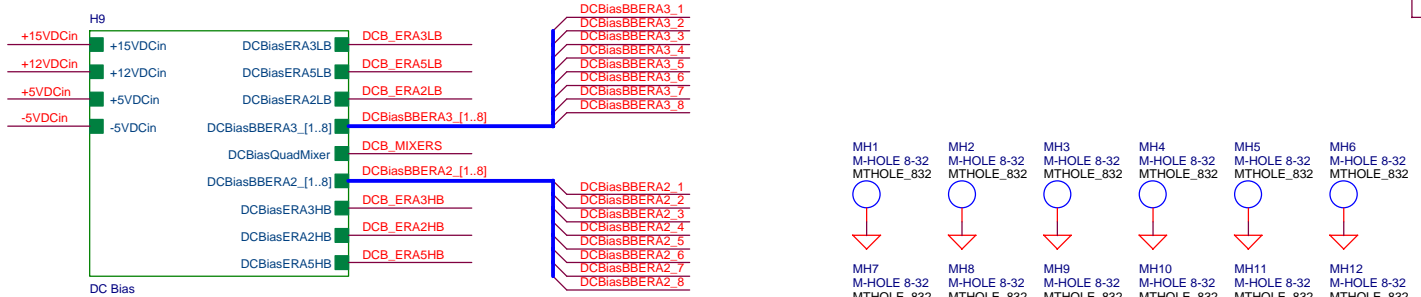
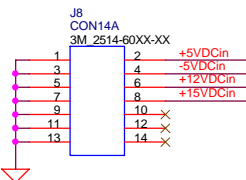
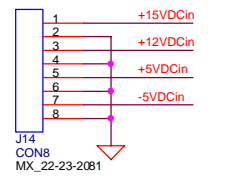
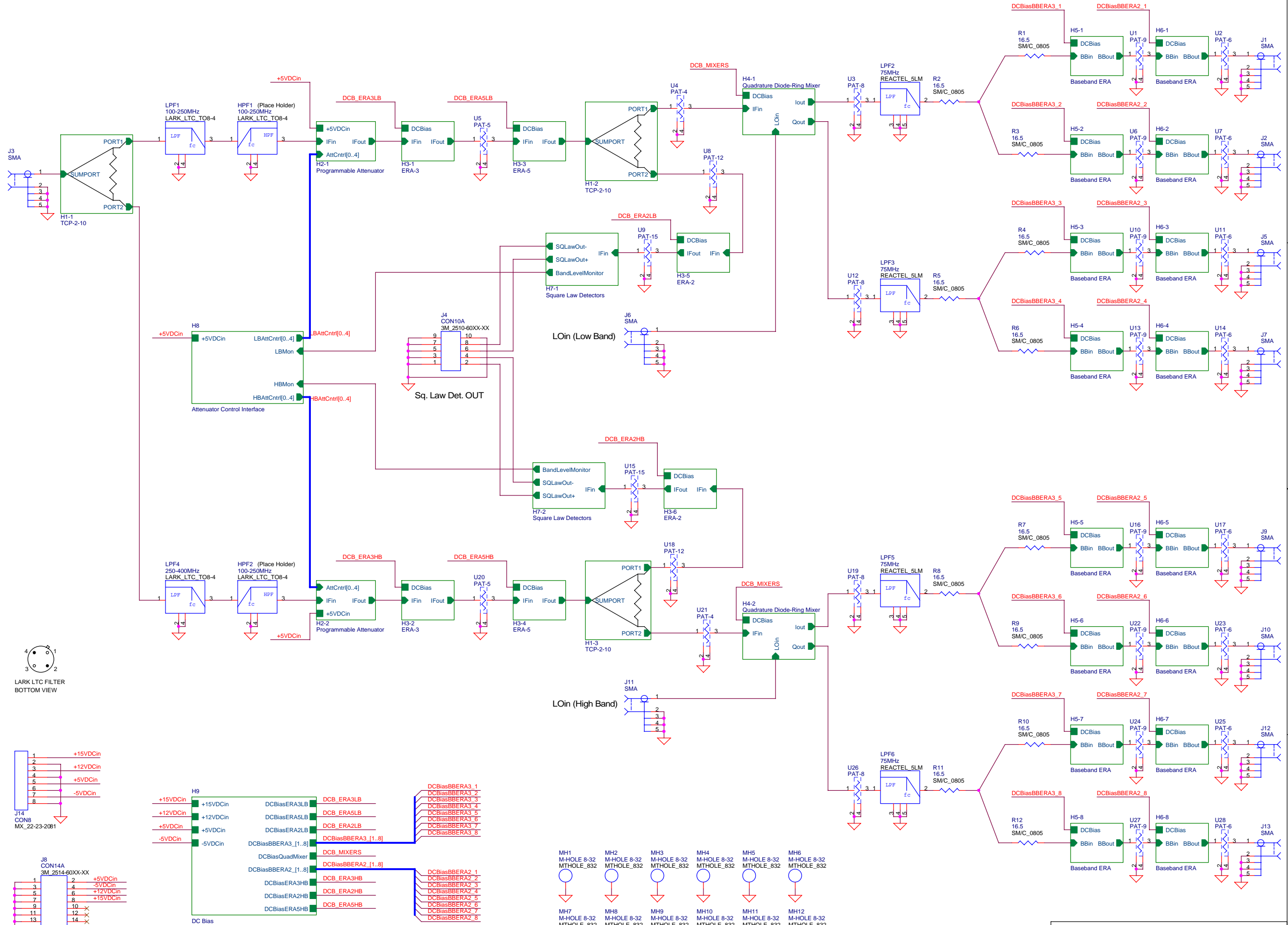


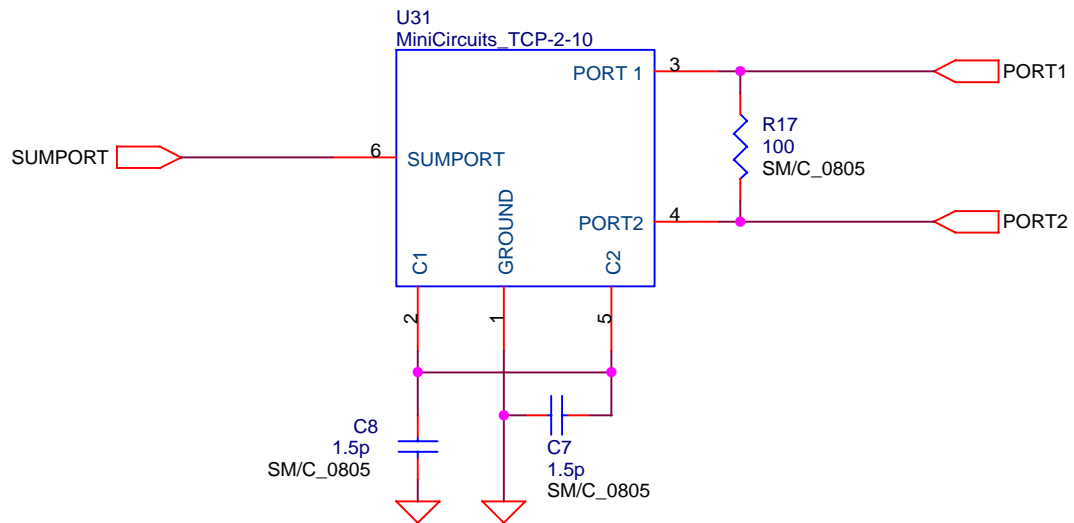
FIGURE 1: EALFA/PALFA BASEBAND MIXER BLOCK DIAGRAM (7th cut) using Ring Diode Demod instead

Dana Whitlow
25 Oct 2007
TOO_EALFA_ANALOG_7d_FIG_1_rev1.fc7

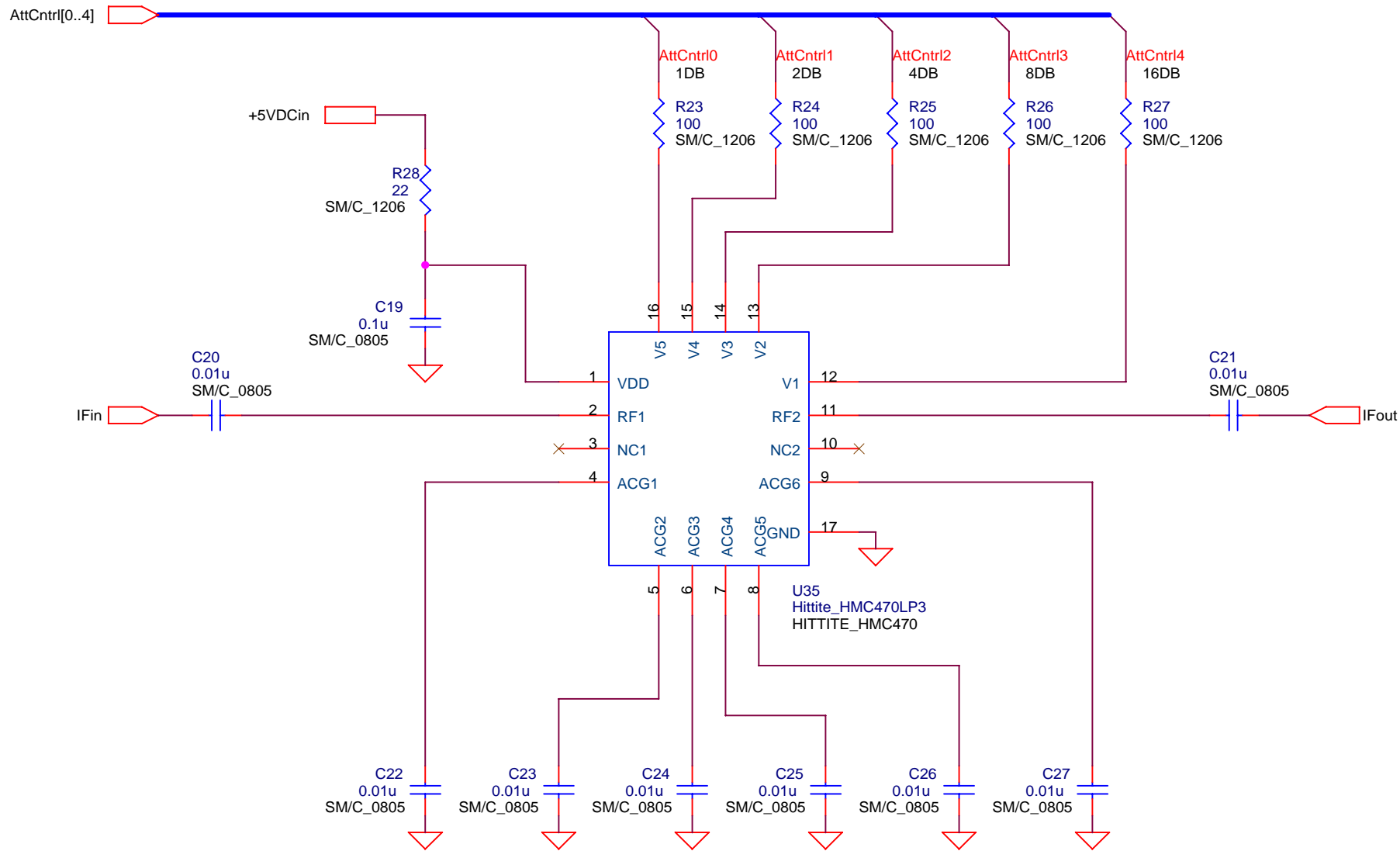
This covers one polarization of 1 ALFA "pixel" (14 req'd)



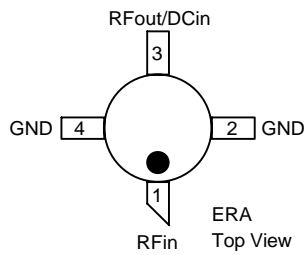
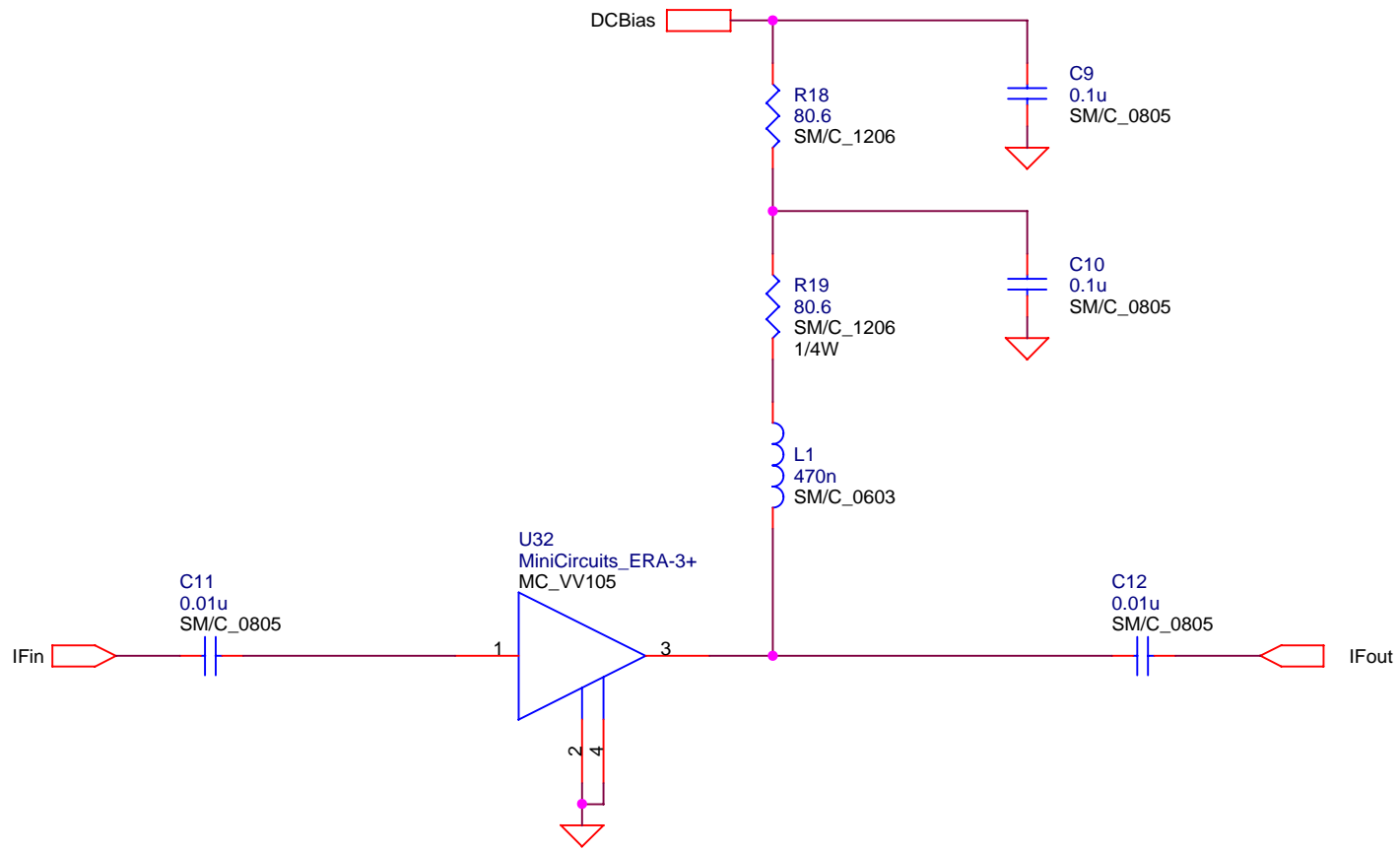
Title: FIGURE 2: Top Level: EALFA ANALOG FRONT END
 Size: C Document Number: <Doc> Rev: X
 Date: Wednesday, April 25, 2007 Sheet: 1 of 40



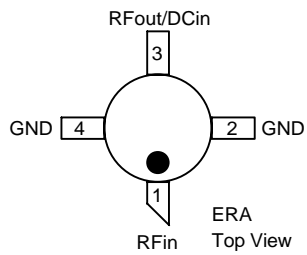
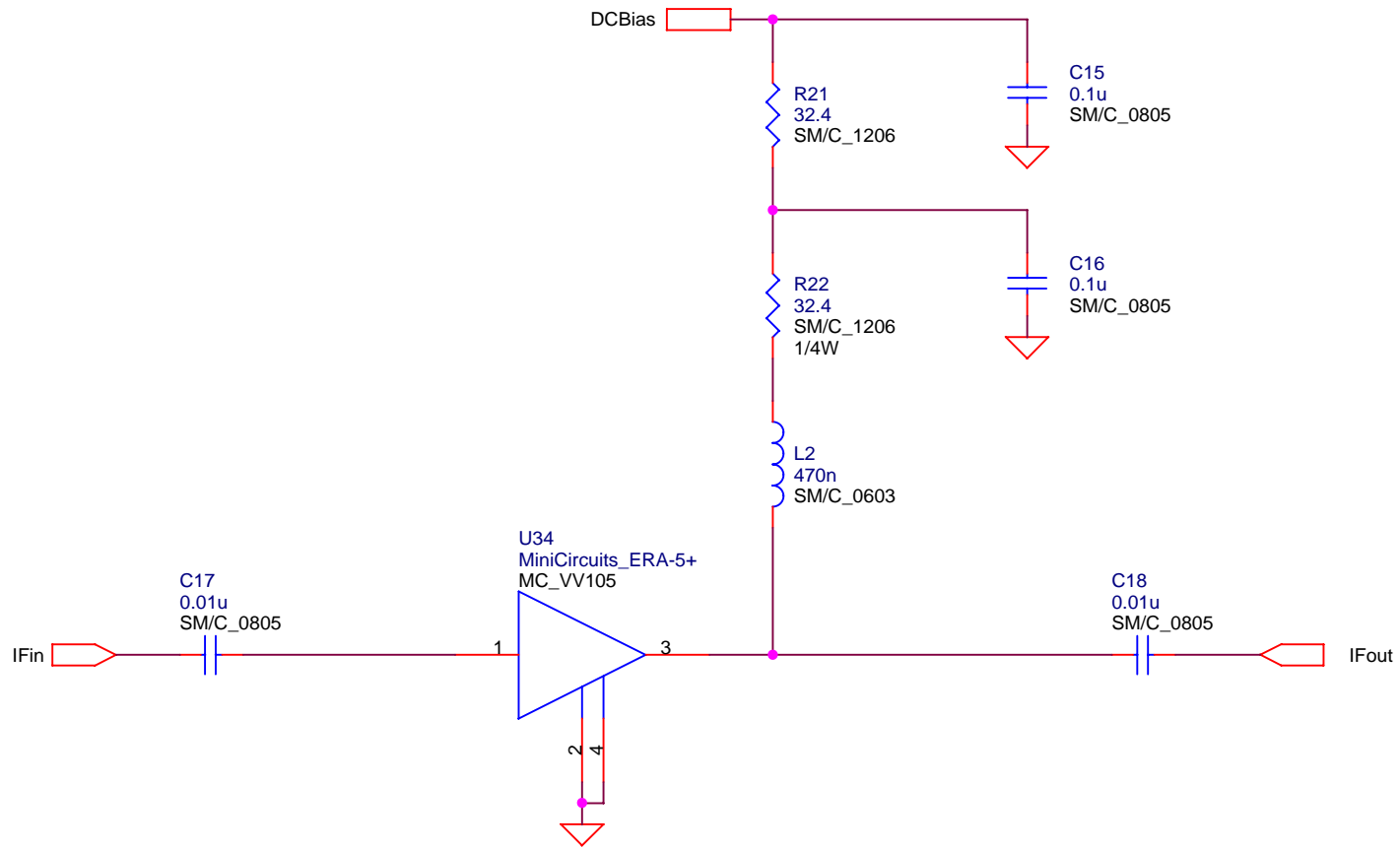
Title		
FIGURE 3: H1-1: TCP-2-10		
Size A	Document Number <Doc>	Rev X6
Date:	Wednesday, March 07, 2007	Sheet 2 of 40



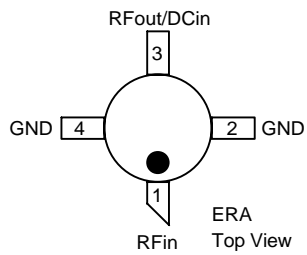
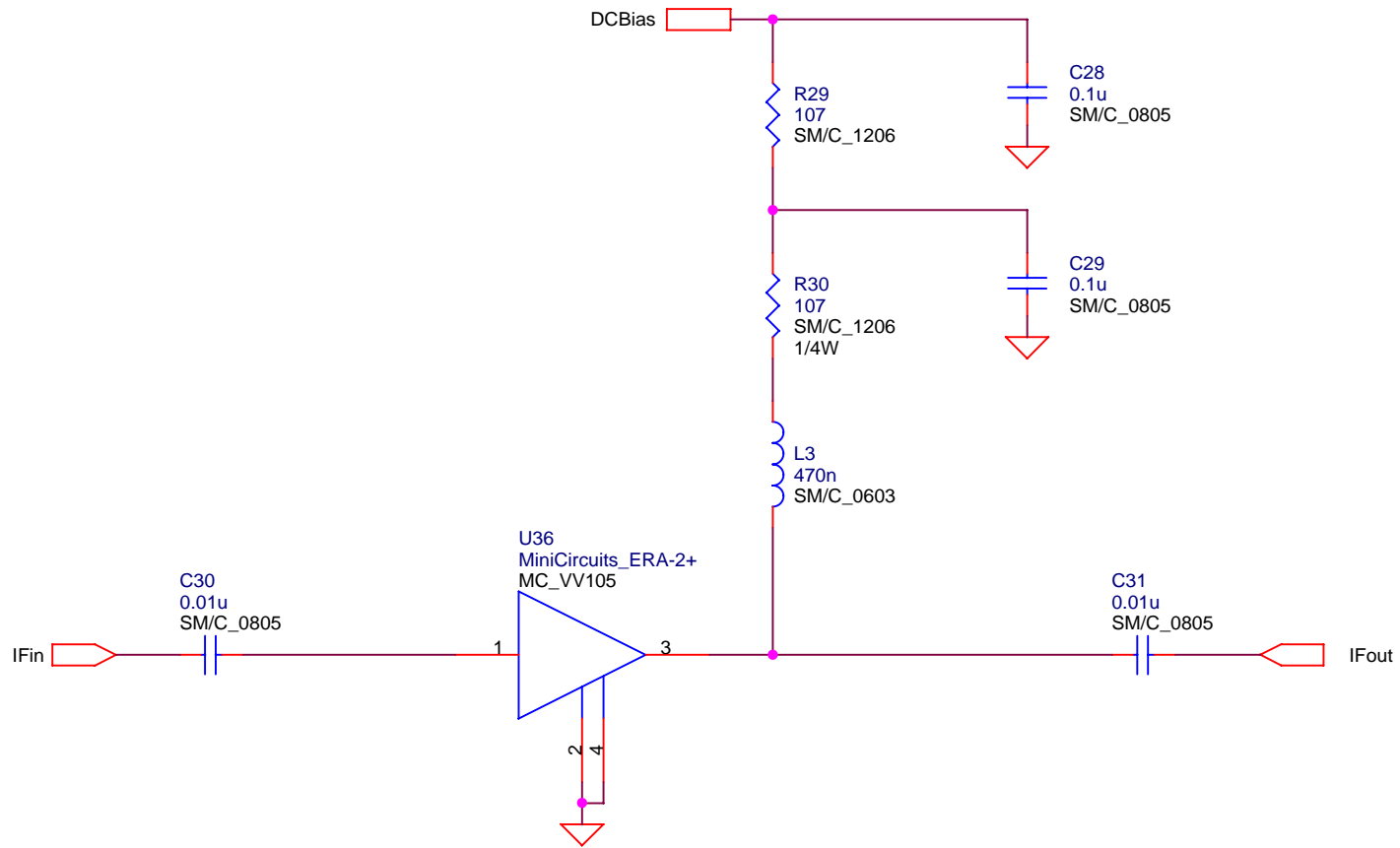
Title		
FIGURE 4: H2-1: Programmable Attenuator		
Size	Document Number	Rev
A	<Doc>	X6
Date:	Friday, April 13, 2007	Sheet 7 of 40



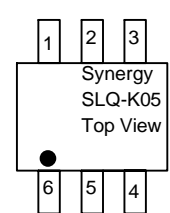
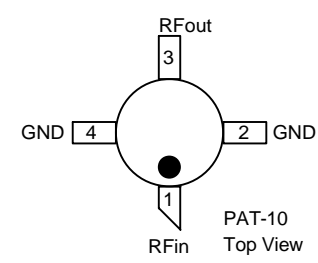
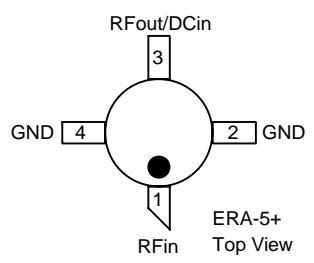
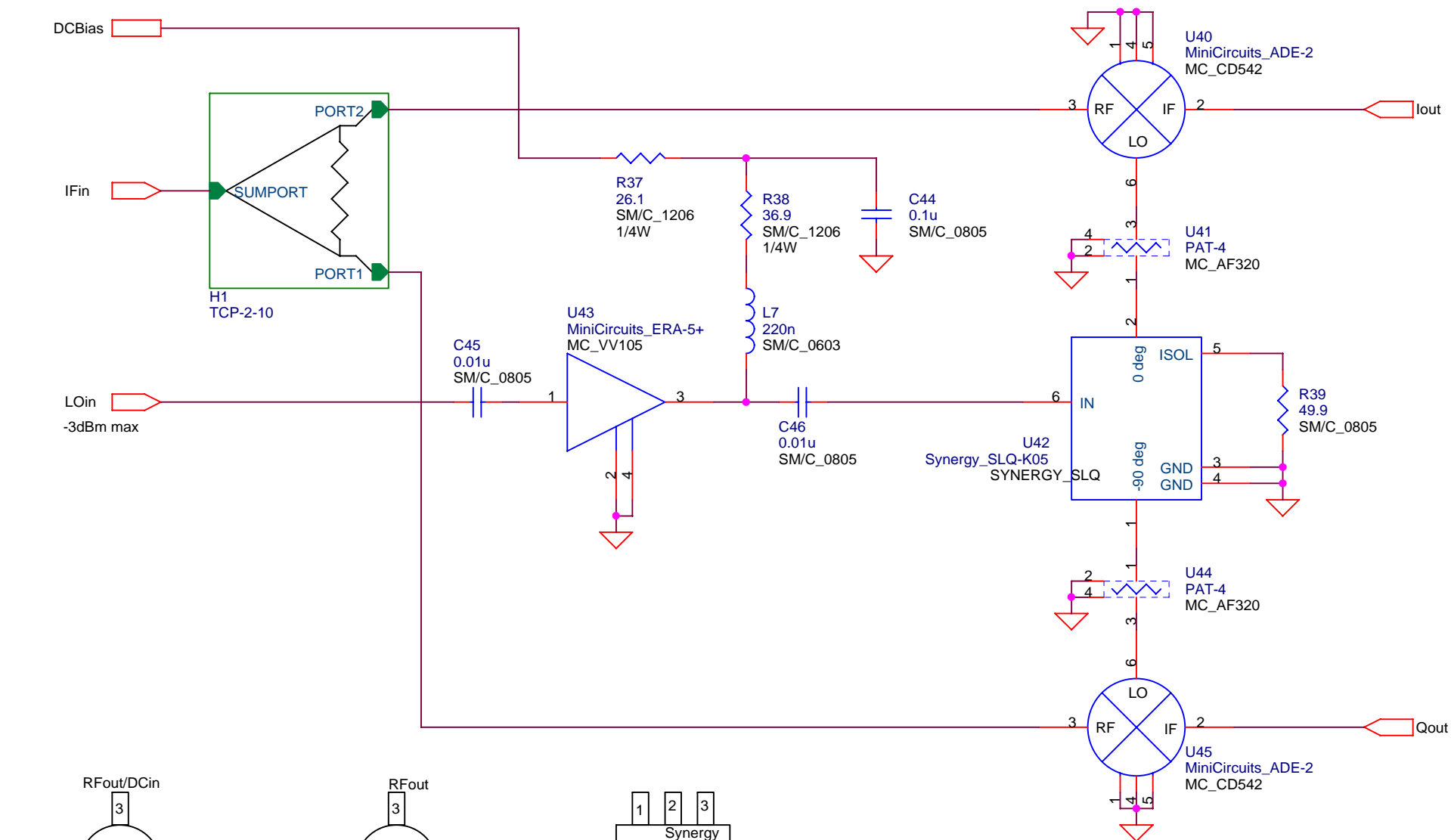
Title		
FIGURE 5: H3-1: IF ERA-3		
Size	Document Number	Rev
A	<Doc>	X6
Date:	Thursday, March 22, 2007	Sheet 9 of 40



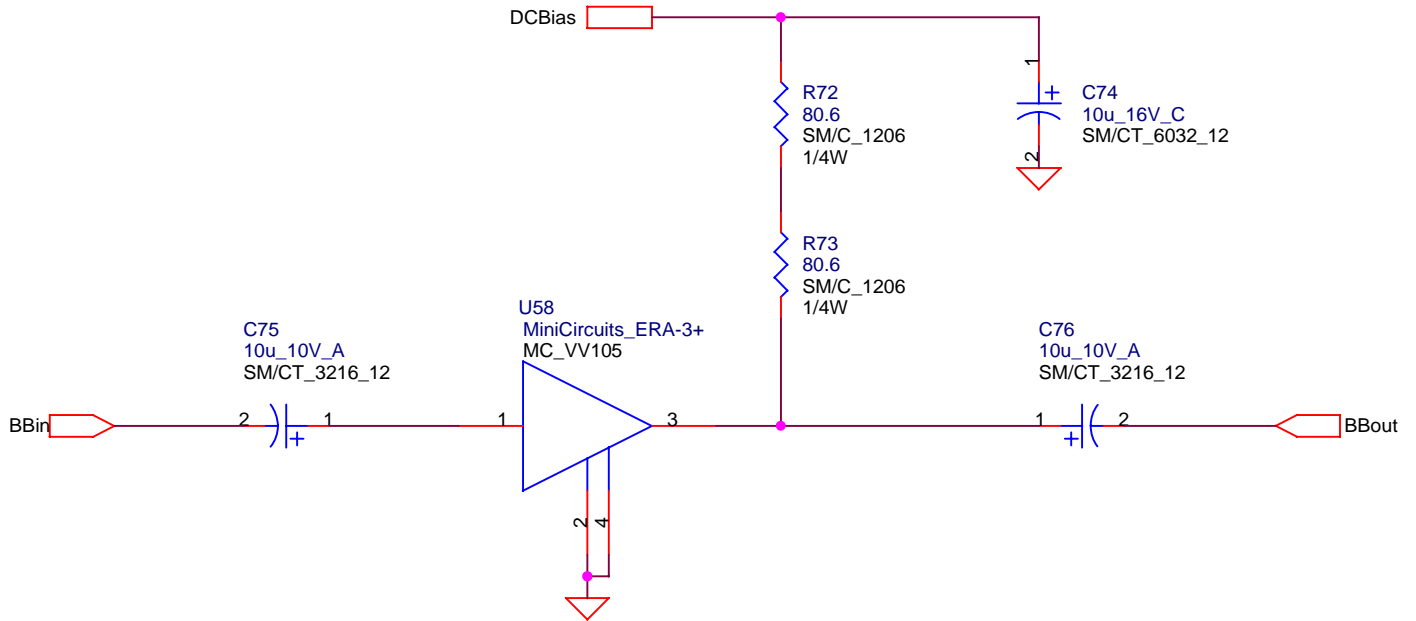
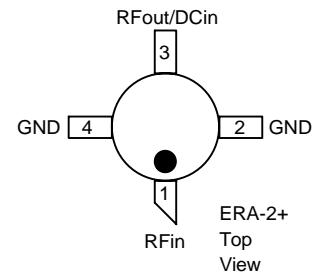
Title		
FIGURE 6: H3-3: IF ERA-5		
Size	Document Number	Rev
A	<Doc>	X6
Date:	Thursday, March 22, 2007	Sheet 11 of 40



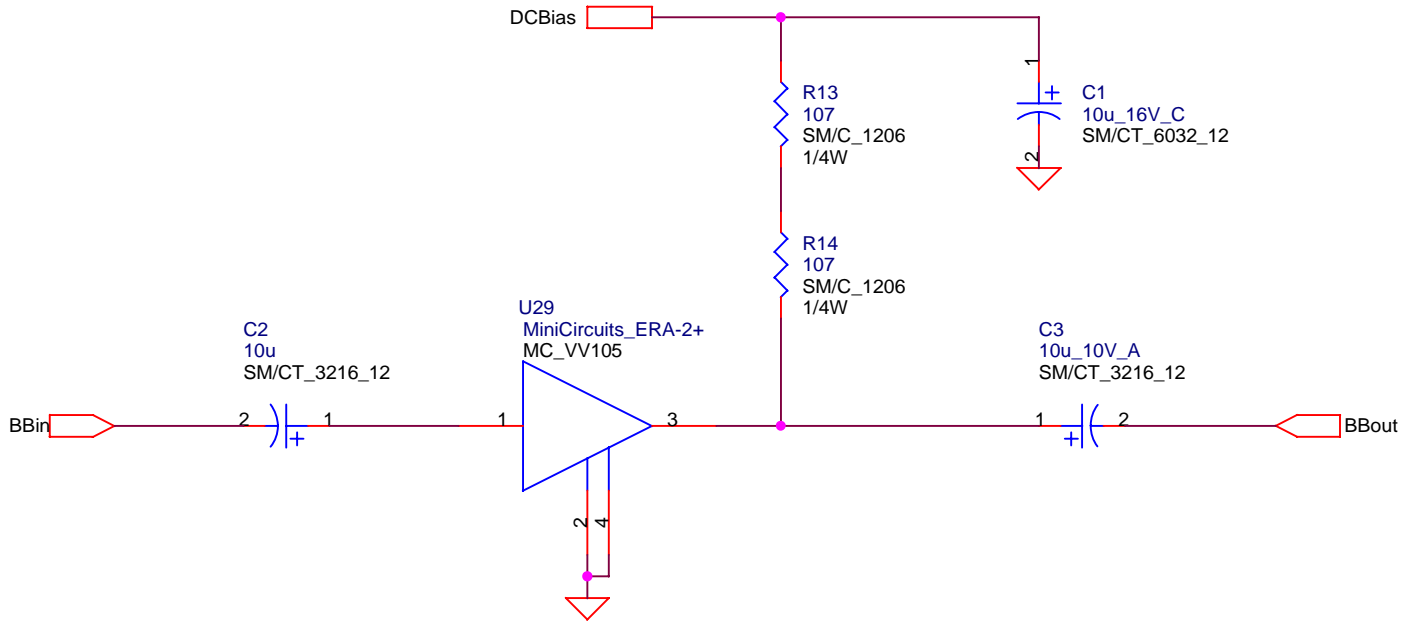
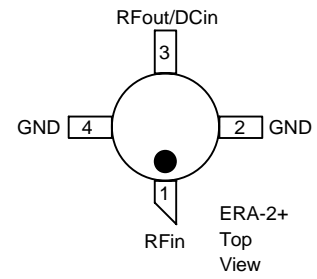
Title		
FIGURE 7: H3-5: IF ERA-2		
Size	Document Number	Rev
A	<Doc>	X6
Date:	Thursday, March 22, 2007	Sheet 13 of 40



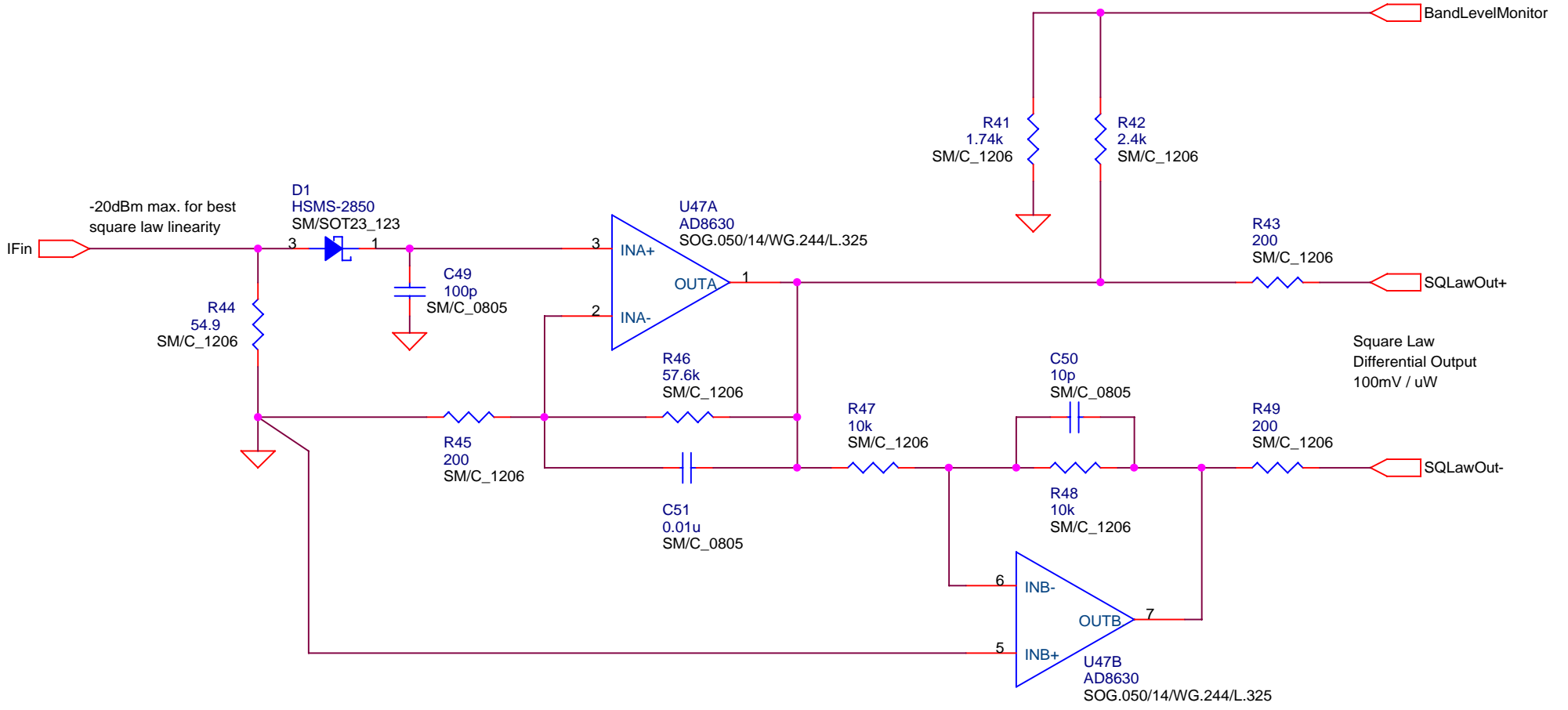
Title		
FIGURE 8: H4-1: Quadrature Diode-Ring Mixer		
Size	Document Number	Rev
A	<Doc>	X6
Date:	Thursday, April 12, 2007	Sheet 15 of 40



Title		
FIGURE 9: H5-1: Baseband Amplifier ERA-3+		
Size	Document Number	Rev
A	<Doc>	X6
Date:	Friday, March 16, 2007	Sheet 17 of 40

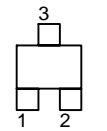


Title		
FIGURE 10: H6-1: Baseband Amplifier ERA-2+		
Size A	Document Number <Doc>	Rev X6
Date:	Friday, March 16, 2007	Sheet 25 of 40



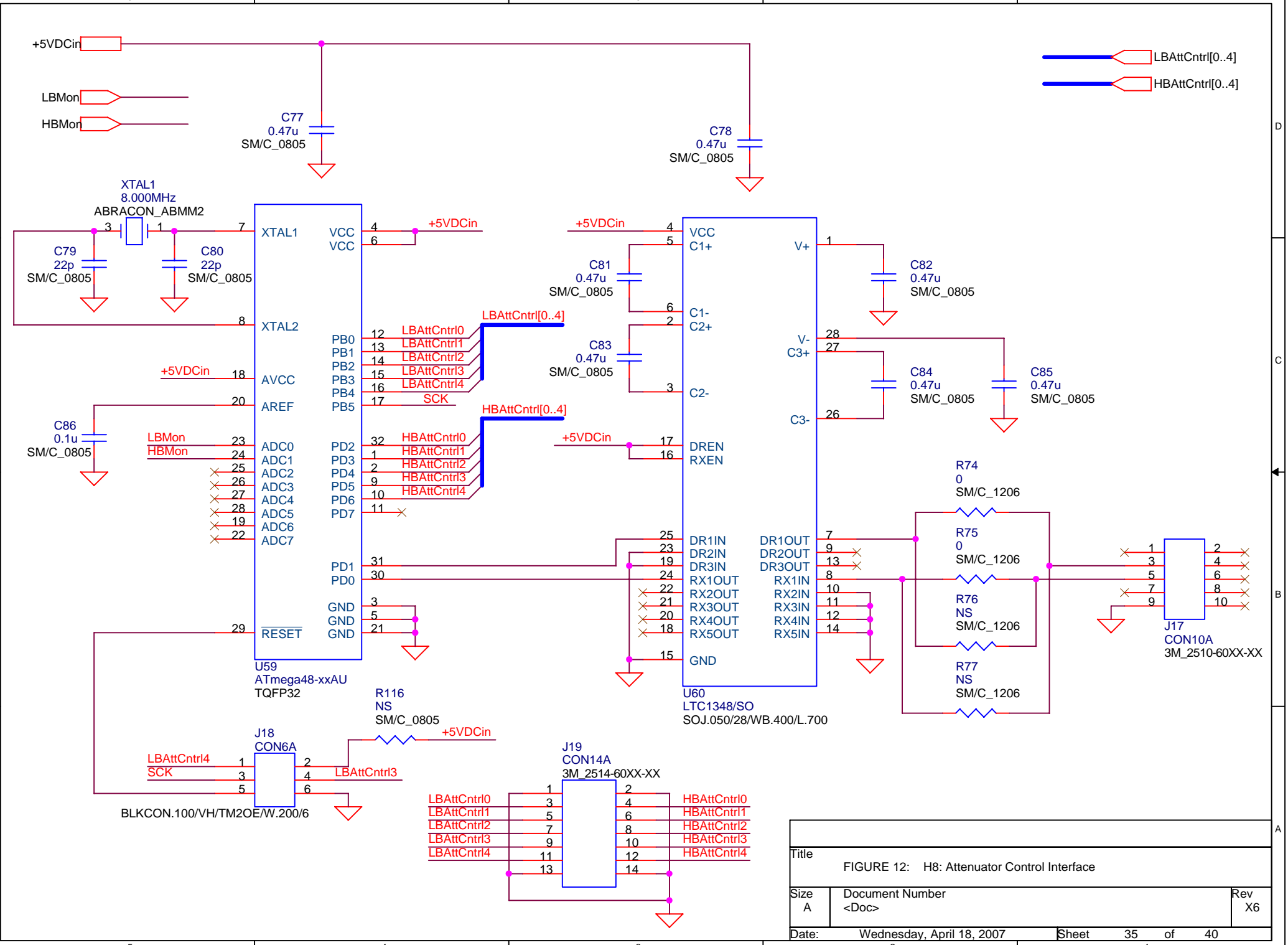
Square Law
Differential Output
100mV / uW

Output common mode voltage is 0V

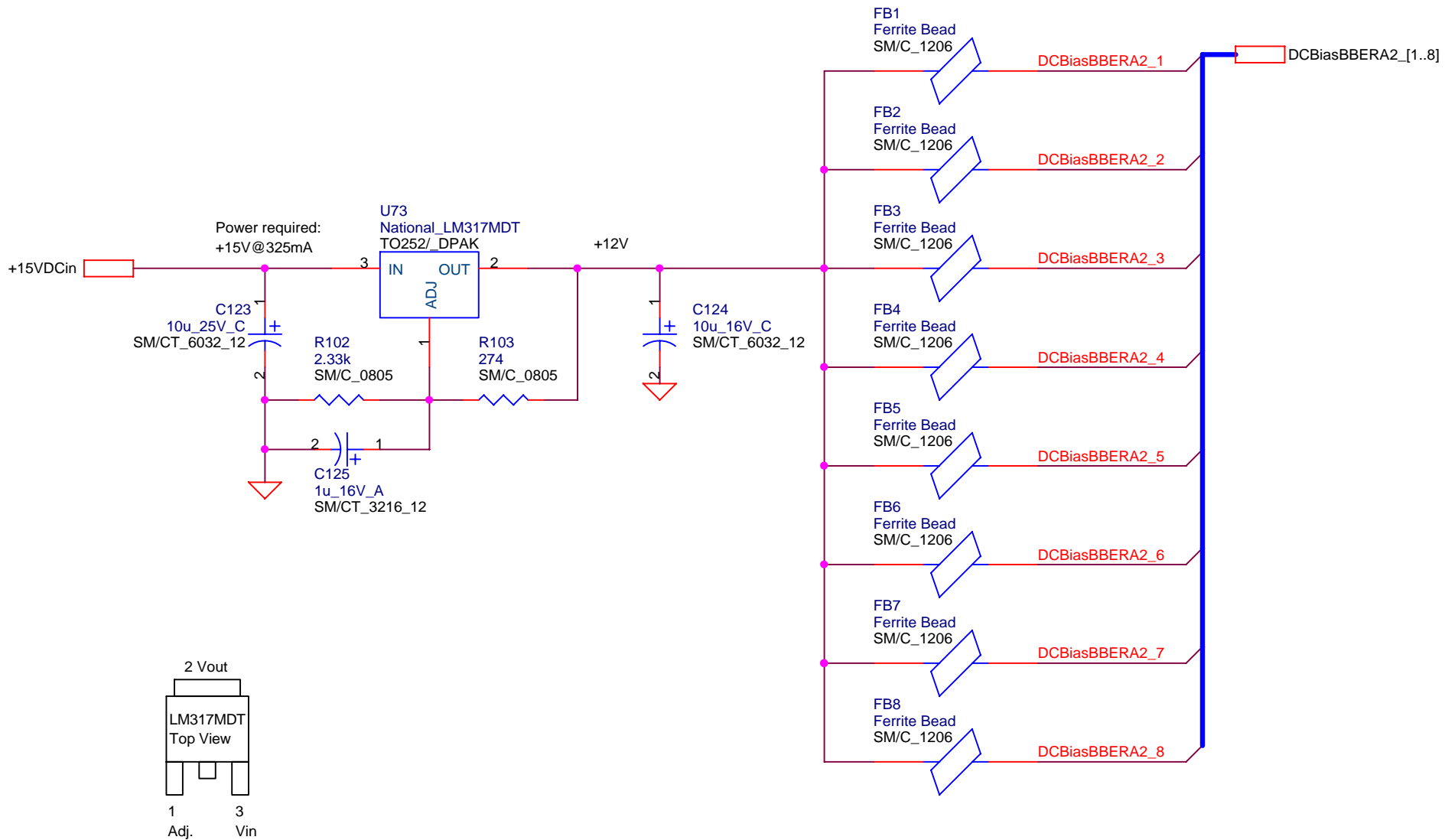


HSMS-2850
TOP VIEW

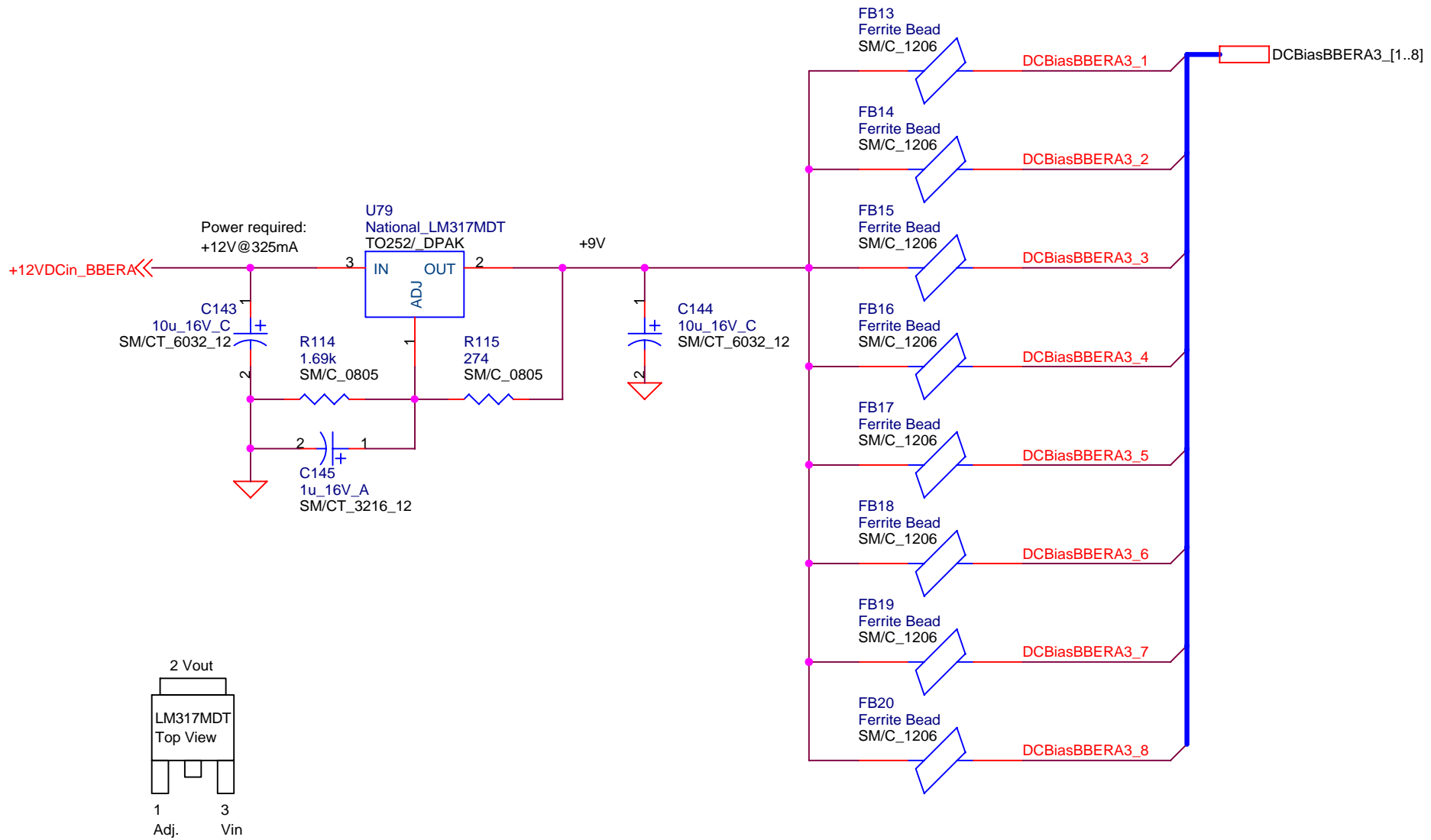
Title		
FIGURE 11: H7-1: Square Law Detectors with Differential Outputs		
Size	Document Number	Rev
A	<Doc>	X6
Date:	Wednesday, March 21, 2007	Sheet 33 of 40



Title		
FIGURE 12: H8: Attenuator Control Interface		
Size	Document Number	Rev
A	<Doc>	X6
Date:	Wednesday, April 18, 2007	Sheet 35 of 40



Title		
FIGURE 13: H9: DC Bias for Baseband ERA-2 Amplifier		
Size	Document Number	Rev
A	<Doc>	X6
Date:	Wednesday, March 21, 2007	Sheet 36 of 40



Title		
FIGURE 14: H9: DC Bias for Baseband ERA-3 Amplifier		
Size	Document Number	Rev
A	<Doc>	X6
Date:	Wednesday, March 21, 2007	Sheet 37 of 40

+12VDCin_ERA

DCBiasERA2LB

DCBiasERA2HB

Power required:
+12V@220mA

U74
National_LM317MDT
TO252/ DPAK

+9V

FB9
Ferrite Bead
SM/C_1206

DCBiasERA3LB

C126
10u_16V_C
SM/CT_6032_12

R104
1.69k
SM/C_0805

R105
274
SM/C_0805

C127
10u_16V_C
SM/CT_6032_12

FB10
Ferrite Bead
SM/C_1206

DCBiasERA3HB

C128
1u_16V_A
SM/CT_3216_12

Power required:
+12V@220mA

U75
National_LM317MDT
TO252/ DPAK

+9V

FB11
Ferrite Bead
SM/C_1206

DCBiasERA5LB

C129
10u_16V_C
SM/CT_6032_12

R106
1.69k
SM/C_0805

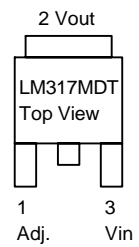
R107
274
SM/C_0805

C130
10u_16V_C
SM/CT_6032_12

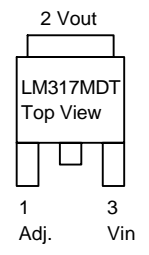
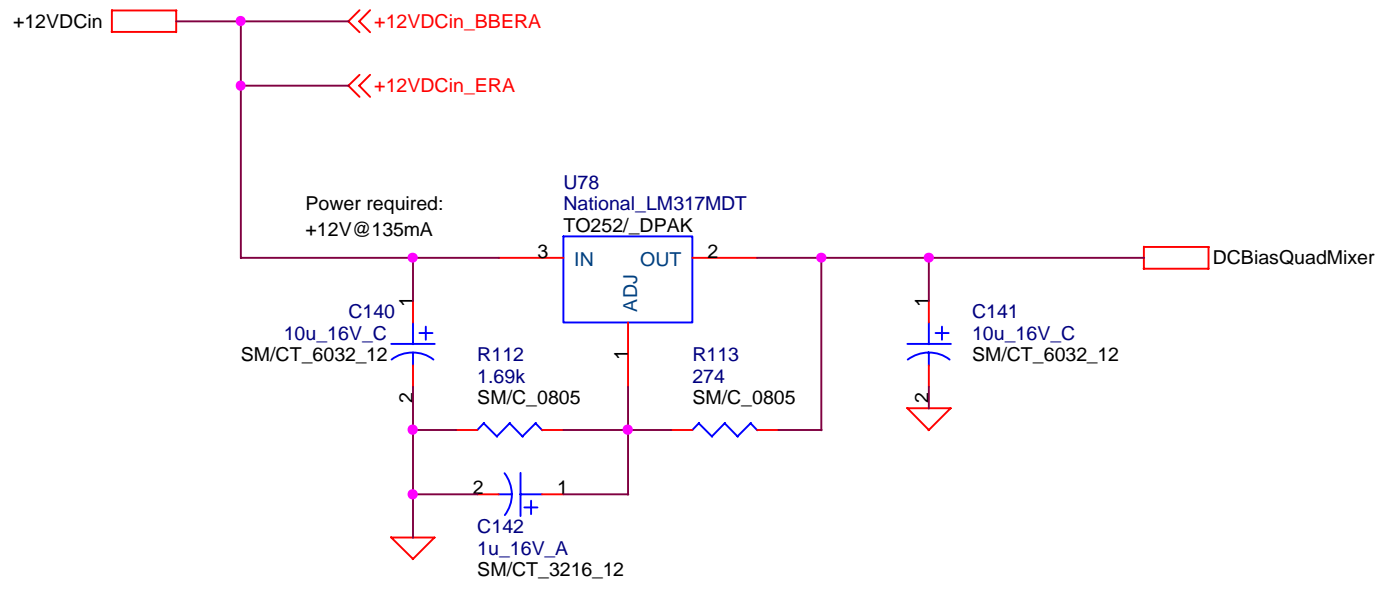
FB12
Ferrite Bead
SM/C_1206

DCBiasERA5HB

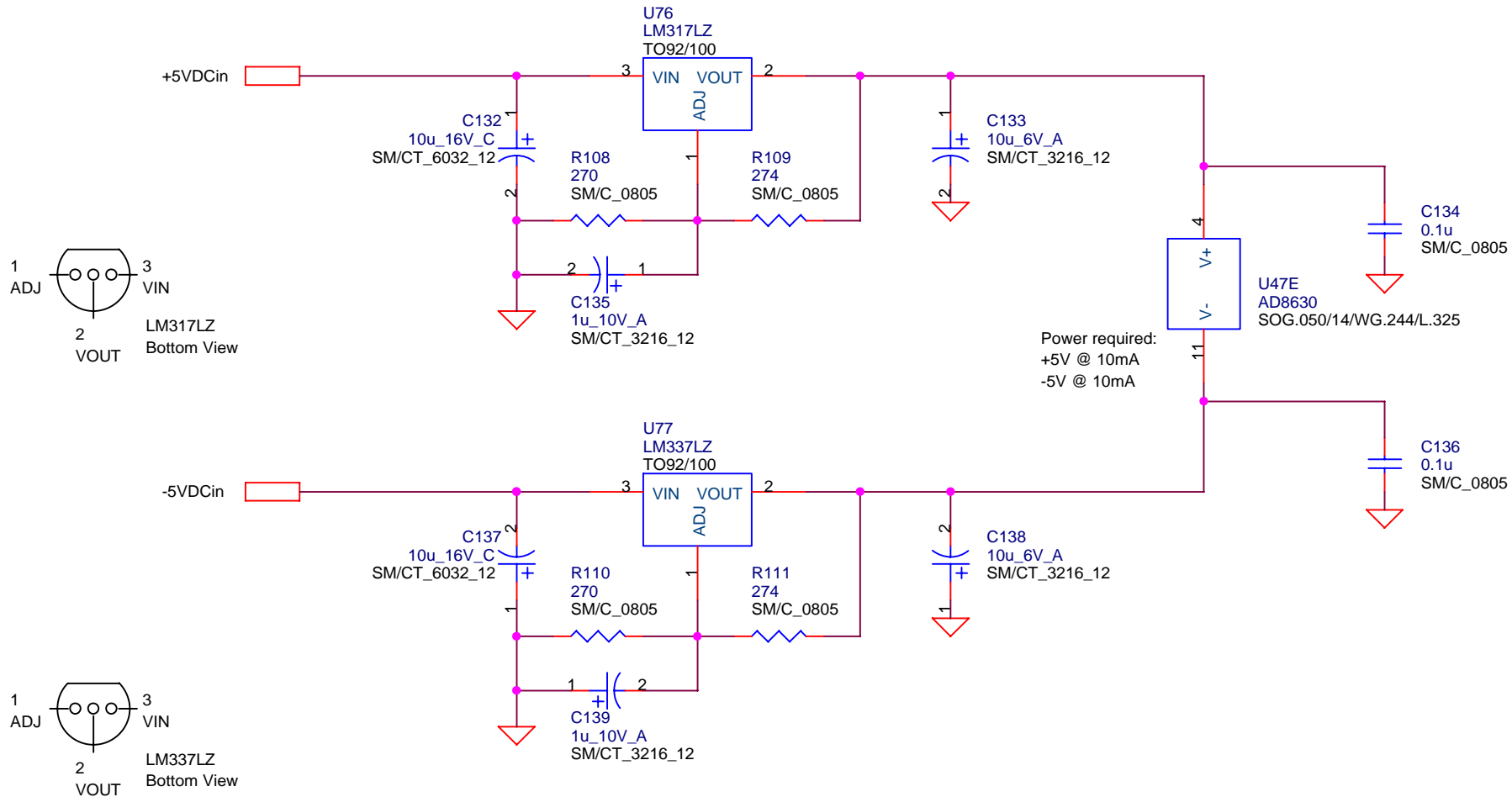
C131
1u_16V_A
SM/CT_3216_12



Title		
FIGURE 15: H9: DC Bias for IF ERA Amplifiers		
Size A	Document Number <Doc>	Rev X6
Date:	Wednesday, April 25, 2007	Sheet 38 of 40



Title		
FIGURE 16: H9: DC Bias for Quadrature Diode-Ring Mixer		
Size A	Document Number <Doc>	Rev X6
Date:	Wednesday, March 21, 2007	Sheet 39 of 40



Title		
FIGURE 17: H9: DC Bias for Square Law Detectors		
Size	Document Number	Rev
A	<Doc>	X6
Date:	Wednesday, March 21, 2007	Sheet 40 of 40