

FPGA P-ALFA backend

GALFA 3rd Meeting
2004-08-29
Arecibo Observatory

Giacomo Comes

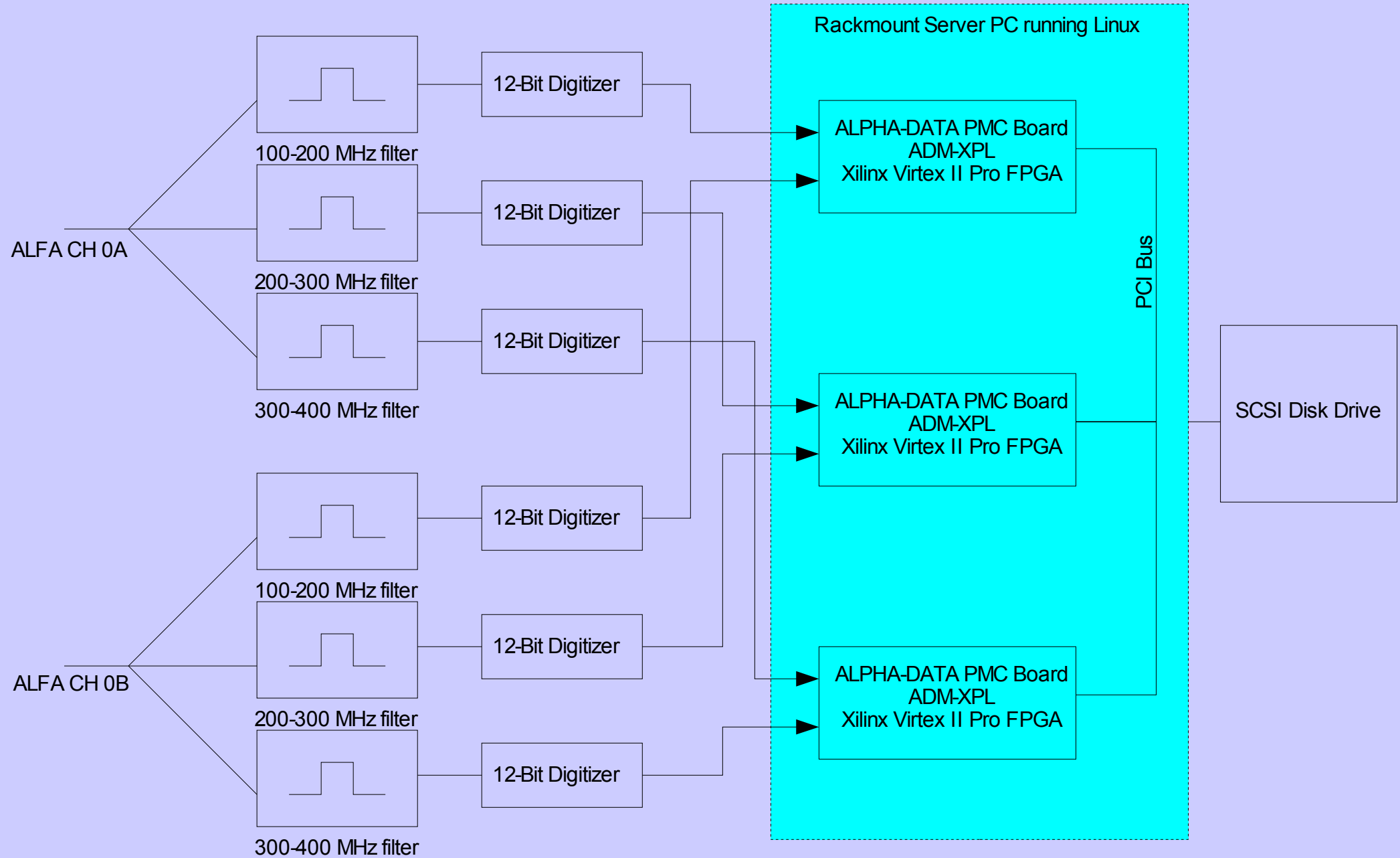
P-Alfa backend requirements

- ◆ Bandwidth 300 MHz
- ◆ Channels 1000 (300 KHz resolution)
- ◆ Input Levels 8 bits (minimum)
- ◆ Output levels 4 bits (software)
after mean subtraction
- ◆ Integration time 64 us (pulsar)
1 ms (continuum)
- ◆ Number of products 1 summed channel (pulsar)
4 (continuum)

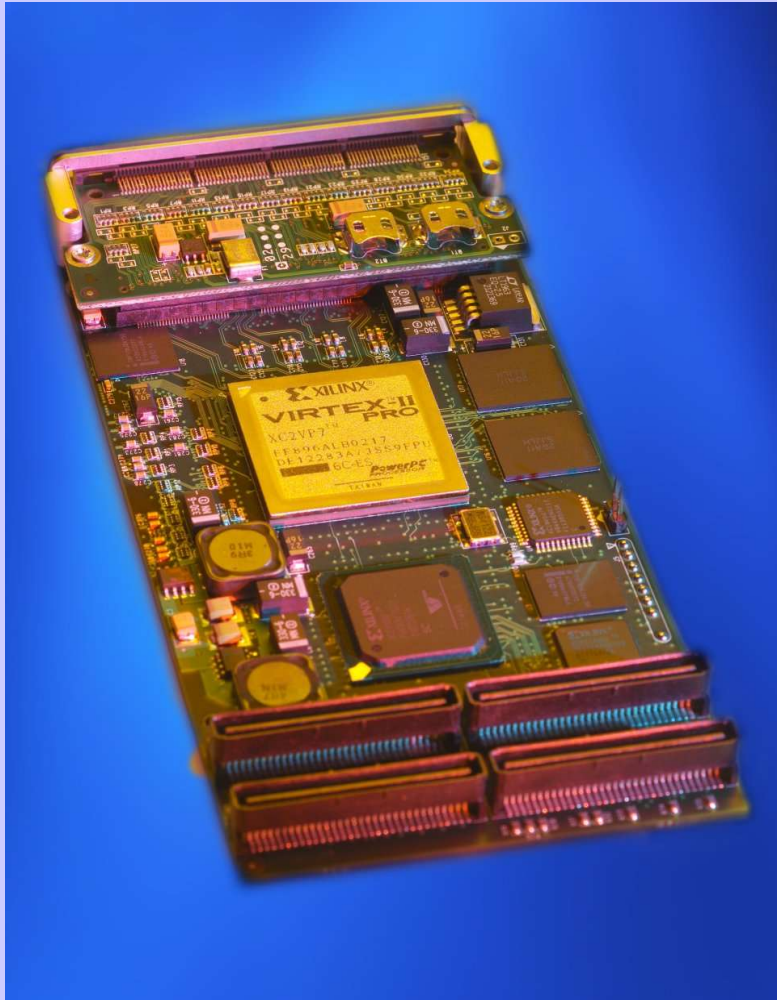
P-Alfa backend implementation

- ◆ Bandwidth 300 MHz
- ◆ Channels 1536 (200 KHz resolution)
- ◆ Input Levels 12 bits
- ◆ Output levels 18 bits (hardware)
flexible (software)
- ◆ Integration time 66.5 us (pulsar)
1 ms (continuum)
- ◆ Number of products 1 summed channel (pulsar)
4 (continuum)

One of Seven ALFA Channels



ALPHA DATA ADM-XPL



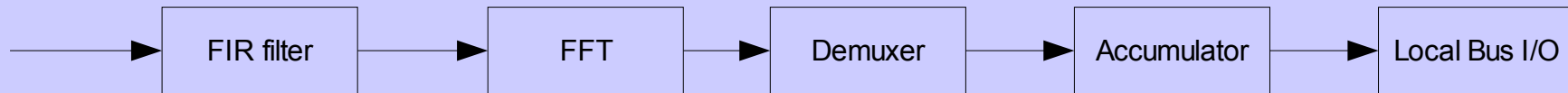
- ◆ PCI Mezzanine card
- ◆ Xilinx Virtex II Pro 2VP20/30
- ◆ 66MHz 64-bit PCI bus
- ◆ Up to 64 LVDS I/O
- ◆ Cost: \$5000

ALPHA DATA products line

Different Xilinx devices supported
Easy scalability

Device	Logic Cells	BRAM	Multipliers
2VP20	20880	1584	88
2VP30	30816	2448	136
2VP70	74448	5904	328
2VP100	99216	7992	444
2VP125	125136	10008	556

FPGA block diagram



- ◆ Polyphase filter
 - ◆ 1024-point pipeline FFT
 - ◆ Sequence demuxer
 - ◆ 22-bit integer accumulator
-
- ◆ 3x7 such modules (worst case)
further optimization may reduce it

Current Status

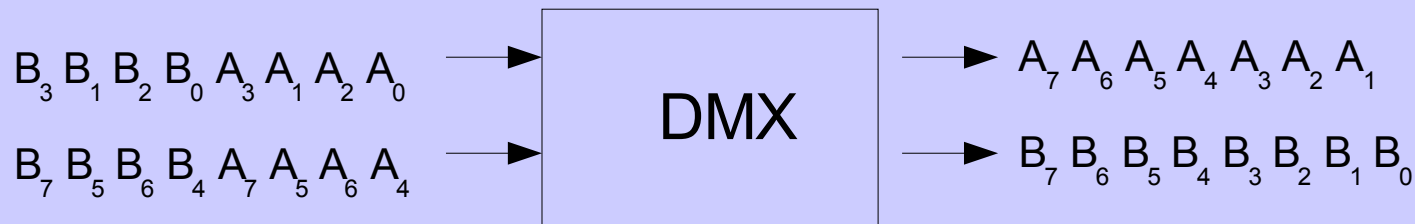
- ◆ The following System Generator block design is done
 - 2^n point – 2 stream pipeline FFT
 - bit-reverse and sequence demuxer
 - Accumulator
 - Alpha Data PCI I/O Buffer
- ◆ Linux kernel driver and library working
- ◆ Test C program working

Pipeline FFT

- ◆ 100% efficiency using two input streams

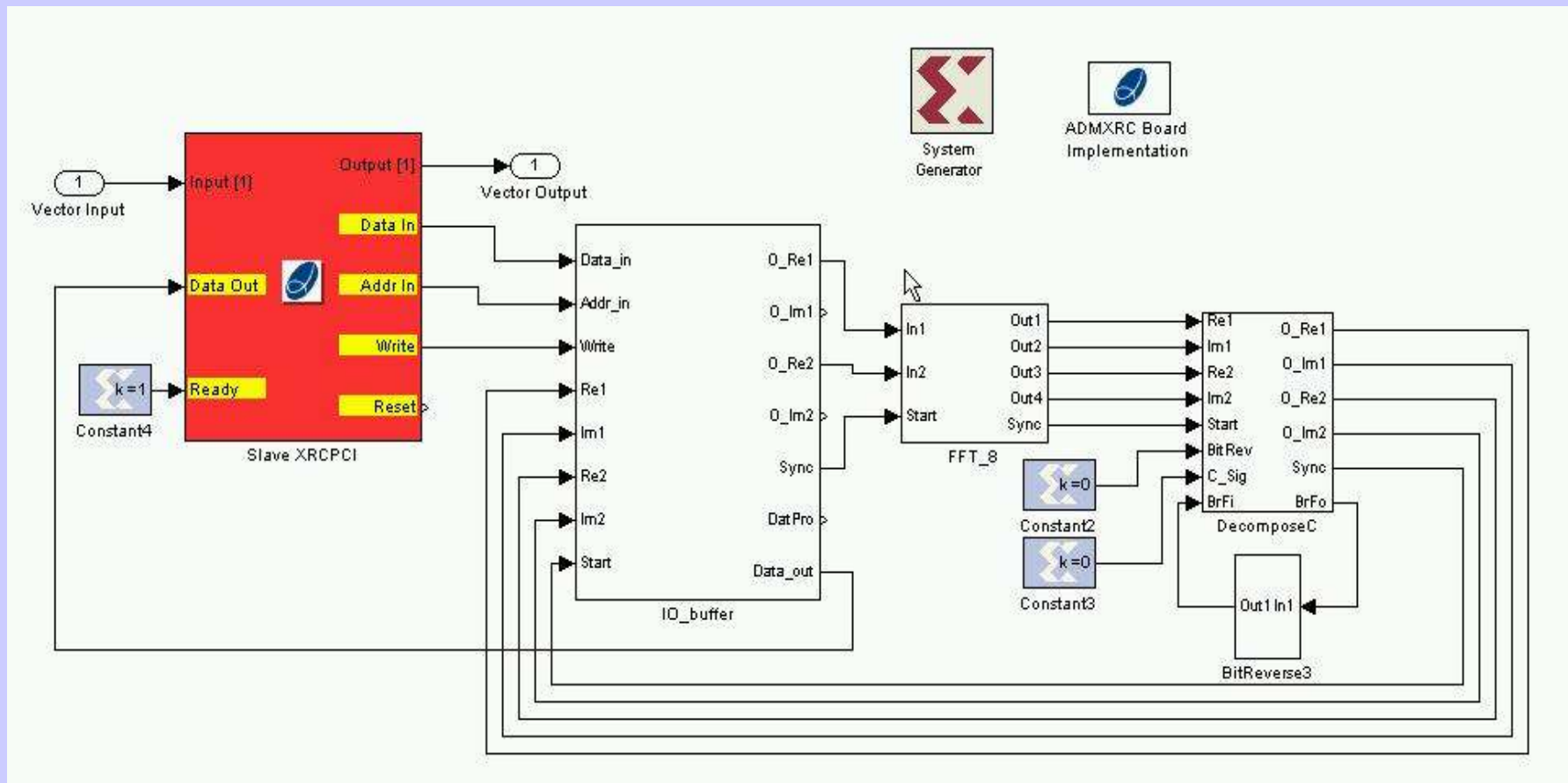


- ◆ bit reverse and sequence demux required

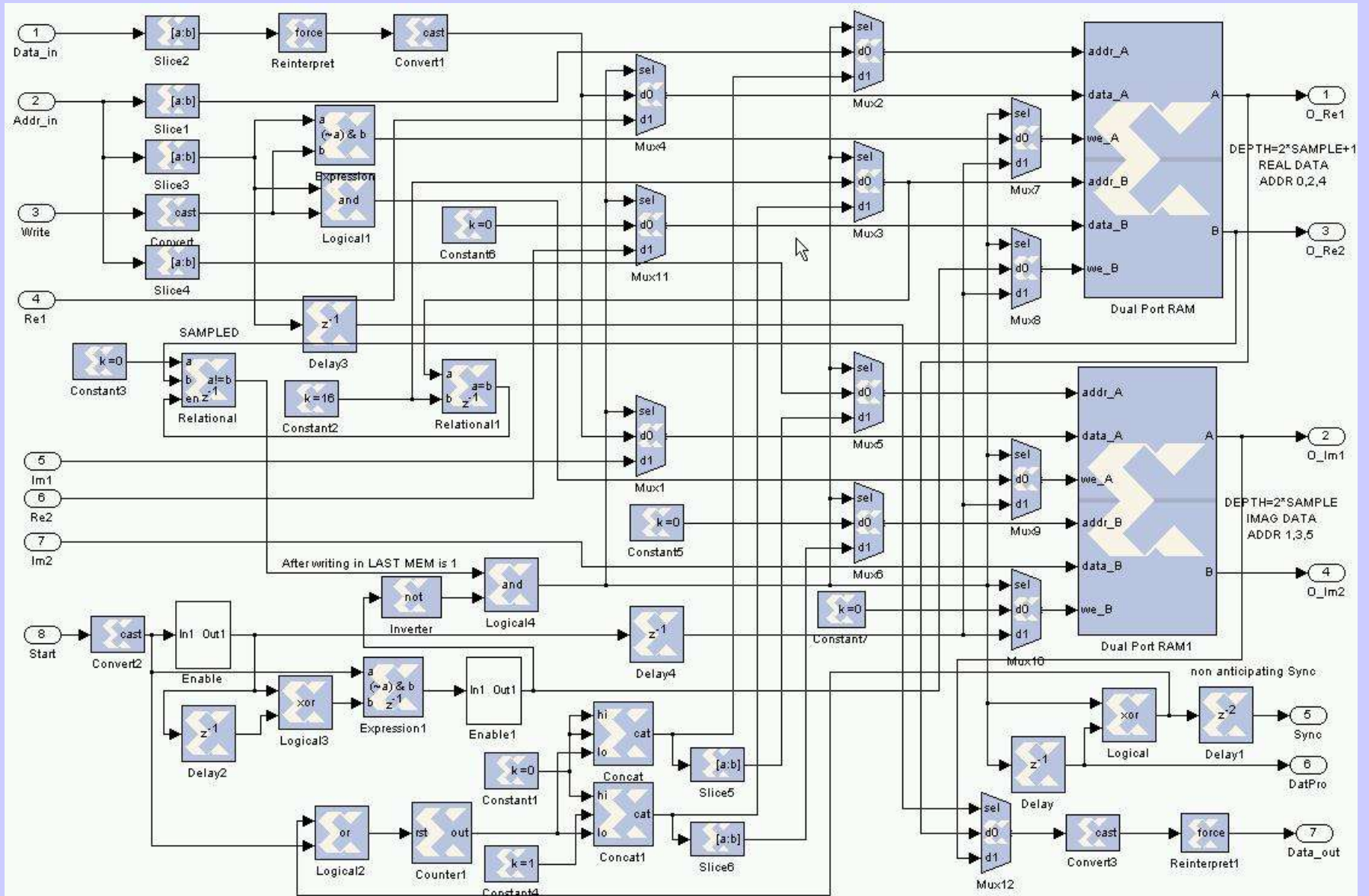


Example test circuit

- ◆ PC to FPGA data write
- ◆ FPGA data processing
- ◆ FPGA to PC data read



I/O buffer circuit



Next Steps

- ◆ Polyphase filter
- ◆ DMA FPGA to PC access