The design of GALFA Quadrature Downconverter

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Specifications:

The goal of the project is to design a quadrature downconverter (QD) that will demodulate an intermediate frequency (IF) signal in the range from 100MHz to 400MHz to base band. There will be a total of 14 QD boards for 7 beams, 2 polarizations per beam, coming from Galactic Arecibo L-band Feed Array (GALFA). The power of the IF signal will be in the range from -25dBm to -10dBm (50Ω load) and will need to be amplified to 0dBm (50Ω load). The demodulated I and Q signal from QB are to be followed by 40 MHz (-3dB point) low-pass image rejection filters with no pass-band ripple, and high stop band attenuation. It is essential that the phase difference between the I and Q demodulated signals at the output does not exceed 3 degrees. The QB will drive 8 bit ADC that will sample at 100Msamples/s.

Block Diagram and Schematic:

Fig.1 illustrates the block diagram of GALFA QD board (load/ADC is not on the board). It also summarizes the gain of each block. The QD board is mainly comprised of three type of electronic components: AD8347 (quadrature demodulator, http://www.analog.com/UploadedFiles/Data_Sheets/53999288331825AD8348_0.pdf), MAX4217 (50 Ω 6dB gain buffer, http://pdfserv.maxim-ic.com/en/ds/MAX4214-MAX4222.pdf), and SETI or Synergy low pass filters. For more information on SETI 7th order Butterworth filter, see P. Monat, D. Werthimer, *The design of 7th order Butterworth low pass filter for GALFA spectrometer application,* June 30, 2004. Synergy Microwave filters are custom made for consumer specifications. Both SETI and Synergy filters are LC ladder based and designed for 124 package pin-out described in the former report.

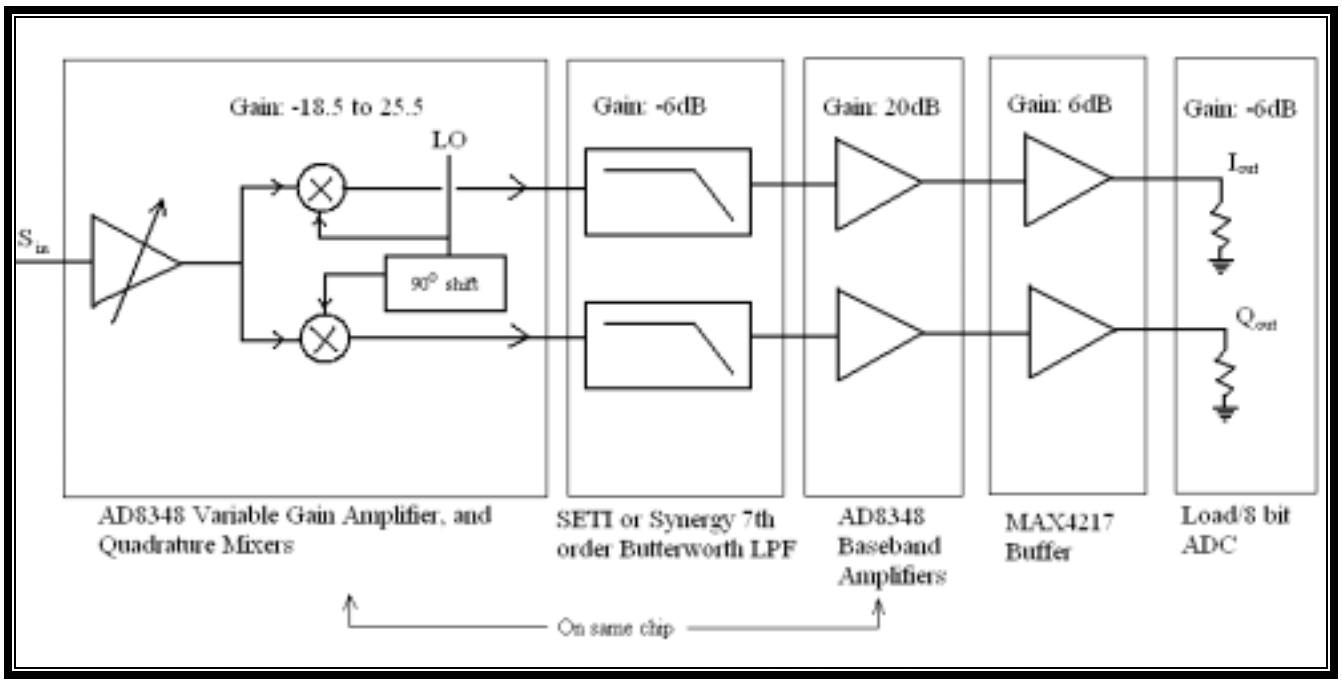


Figure 1: QD block diagram.

Fig.2 shows the QD board schematic. Both AD8348 and MAX4217 are designed to operate on single supply where V_s=5.0V. The power pins of AD8348 (pins 2, 12, 20) are decoupled with 0.1uF and 100pF capacitors. MAX 4217 is decoupled with 0.1uF capacitor at pin 8. Pins 7, 22, 27 on AD8348 are power pins and they are tied to ground.

The VGA on AD8348 needs to be driven differentially. To present a broadband 50Ω load to a single ended driver, a 174Ω resistor is put in series with pin 11, and a 57.6Ω resistor is shunted to ground. The differential inputs (pins 10 and 11) are bypassed with 1000pF caps. The VGA control voltage is tied to pin 17

and decoupled by a 0.1uF cap. For testing purposes, a 10kΩ resistor from voltage supply is tied to 10kΩ potentiometer that goes to ground. In operation, a DAC will drive pin 15. That is why a 3 pin jumper is placed between 10kΩ potentiometer and DAC input.

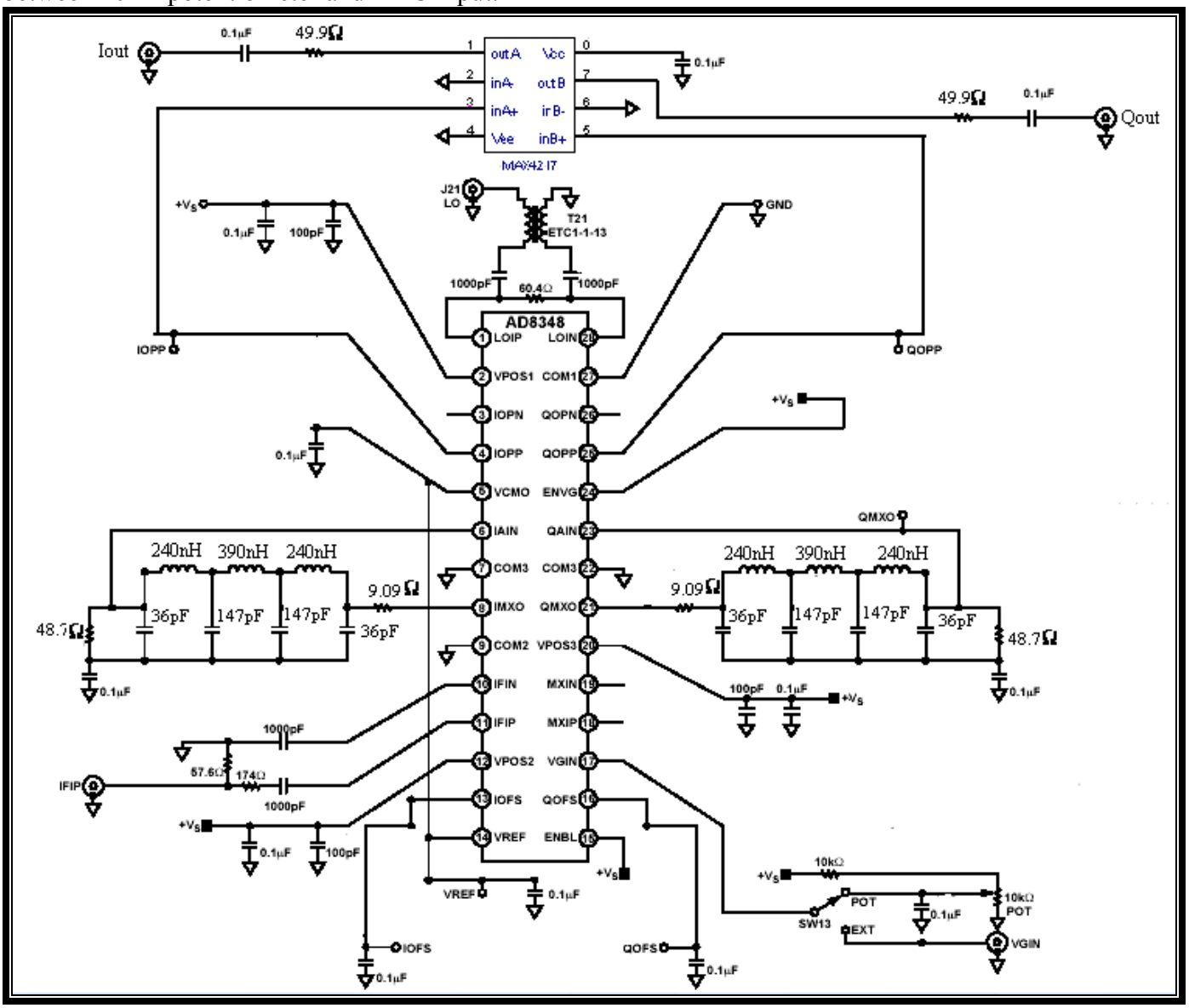


Figure 2: QD schematic

ETC1-1-13 (balun) transforms the single ended local oscillator (LO) input (at twice the carrier frequency) to a differential driver that feeds pin 1 and 28. LO drives pin 4 on ETC1-1-13, pin 5 is grounded, and pins 3 and 4 are the outputs. To present a 50Ω load to the LO driver, a 60.4Ω resistor is tied shunt to pin 1 and 28. Pins 1 and 28 are bypassed by 1000pF capacitors.

The voltage input to pin 5 (on AD8348) sets the common mode output voltage for the base-band amplifiers in AD8348. The 1V voltage reference in 14 is hooked up to pin 5 and it is decoupled to ground by a 0.1uF cap. To enable the voltage reference, tie pin 15 to power supply (V_s). The 2 amp buffer, MAX4217, is driven single ended by pins 4[I_{out}] and 25[Q_{out}] on AD8348 (pins 3 and 26 are left open). Pin 4 and 25 on AD8348 drive pin 3 and 5 on MAX4217, respectively. Pins 2, 6 on MAX4217 are grounded for gain of two configuration (pin 4 is grounded for power). Because the common mode output from the AD8348 base-band amplifiers is 1, and MAX4217 has a gain of 2, the common mode output of the I and Q channels on MAX4217 is 2V.

Pins 8 and 21 are the I and Q channel outputs of the AD8348 mixer. Their output resistance is 40Ω. Because the SETI low pass filter was designed for input/output of 49 ohms, a 9.09Ω resistor is put in series with

the output of each channel. Because the I and Q channel inputs (pins 6 and 24, respectively) of base-band amplifiers present high input impedance, a 48.7Ω resistor is tied to 0.1uF cap and then to ground. 0.1uF cap is placed between the 48.7Ω resistor and ground to prevent high DC current (that the VGA cannot supply).

AD8348 allows the user to disable the VGA by tying pin 24 to ground, and driving the mixers differentially though pins 18 and 19. Because this design utilizes the VGA, pin 24 is tied to power supply (V_s), and pin 18 and 19 are left open. Pins 13 and 16 are I and Q channel offset nulling inputs. The DC offset is nulled by decoupling pins 13 and 16 to ground with 0.1uF capacitors.

Layout and Assembly:

Table 1 summarizes the part references on the QD board schematic and layout. These are the names seen on the silkscreen of the QD board (potentiometer is not seen on the silkscreen). This table is essential for assembly of the board. Notice that the parts parked with a star are used in I/Q signal path. To have I/Q phase difference with 3 degrees, these parts should have 1% tolerance. Because the best tolerance for 0.1uF capacitors is 5% (unless 1% tolerance can be found), these capacitors should be pair matched using a capacitor meter and only then installed (C17/C19 and C18/C20).

All parts except MAX4217 were purchased from Digikey. MAX4217 parts were purchased from Maxim-IC.

On Board Part Reference	Value	Size/Package	Precision
U6	28 pin Downconverter (AD8348)	TSSOP (RU-28)	NA
U7	5 pin transformer (ETC1-1-13)	SM-22	NA
U13	8 pin buffer (MAX4217)	8L uMAX/uSOP	NA
C1	1000pF	805	5%
C2	1000pF	805	5%
C3	0.1uF	603	5%
C4	100pF	603	5%
C5	0.1uF	603	5%
C6	100pF	603	5%
C7	0.1uF	603	5%
C8	100pF	603	5%
C9	1000pF	805	5%
C10	1000pF	805	5%
C11	0.1uF	603	5%
C12	0.1uF	603	5%
C13	0.1uF	603	5%
C14	0.1uF	603	5%
C15	0.1uF	603	5%
C16	0.1uF	603	5%
C17*	0.1uF (pair matched)	805	Matched to C19 with 1%
C18*	0.1uF pair matched	805	Matched to C20 with 1%
C19*	0.1uF pair matched	805	Matched to C17 with 1%

C20*	0.1uF (pair matched)	805	Matched to C18 with 1%
R1	60.4Ω	1206	1%
R2	10kΩ Potentiometer	through hole	under 20%
R3	174Ω	1206	1%
R4	57.6Ω	1206	1%
R5	Not on board		
R6	Not on board		
R7*	9.09Ω	805	1%
R8*	9.09Ω	805	1%
R9	Not on board		
R10	Not on board		
R11*	49.9Ω	805	1%
R12*	49.9Ω	805	1%
R13*	48.7Ω	805	1%
R14*	48.7Ω	805	1%
R15	10kΩ	805	5%
J1	Right angle SMA	Right angle bulkhead jack	NA
J6	Right angle SMA	Right angle bulkhead jack	NA
J8	Right angle SMA	Right angle bulkhead jack	NA
J9	Right angle SMA	Right angle bulkhead jack	NA
J10	10 pin connector	2 row, 100 mil spacing	NA
SW1	3 pin jumper	1 row, 100 mil spacing	NA

Table 1: Parts, values, sizes, and tolerances

Decoupling capacitors should be placed as close to the power-supply pins as possible, and 100pF caps would be placed closer than 0.1uF caps.

IF input and LO input are high frequency, and therefore behave like transmission lines. To prevent reflection, IF and LO copper trances are made to be 50Ω (on 62.5 mil FR4, that is 105 mils wide). Wide 1205 resistors terminate these wide copper trances. Because the demodulated I/Q signals are relatively low frequency (under 50MHz), 50Ω wide traces are not used.

Note that 3 pin jumper, SW1, determines whether $V_{control}$ for the VGA comes from the potentiometer/resistive divider or the DAC. For potentiometer control (for testing), the jumper needs to connect the center pin and the pin closer to the potentiometer. For DAC control, the connect the center pin and the pin closer to 10 pin connector.

The I and Q channel traces were length match to less than 1 mil to insure a good quadrature phase at the output.

The board was manufactured by Advanced Circuits, and the parts were assembled by Digicom.

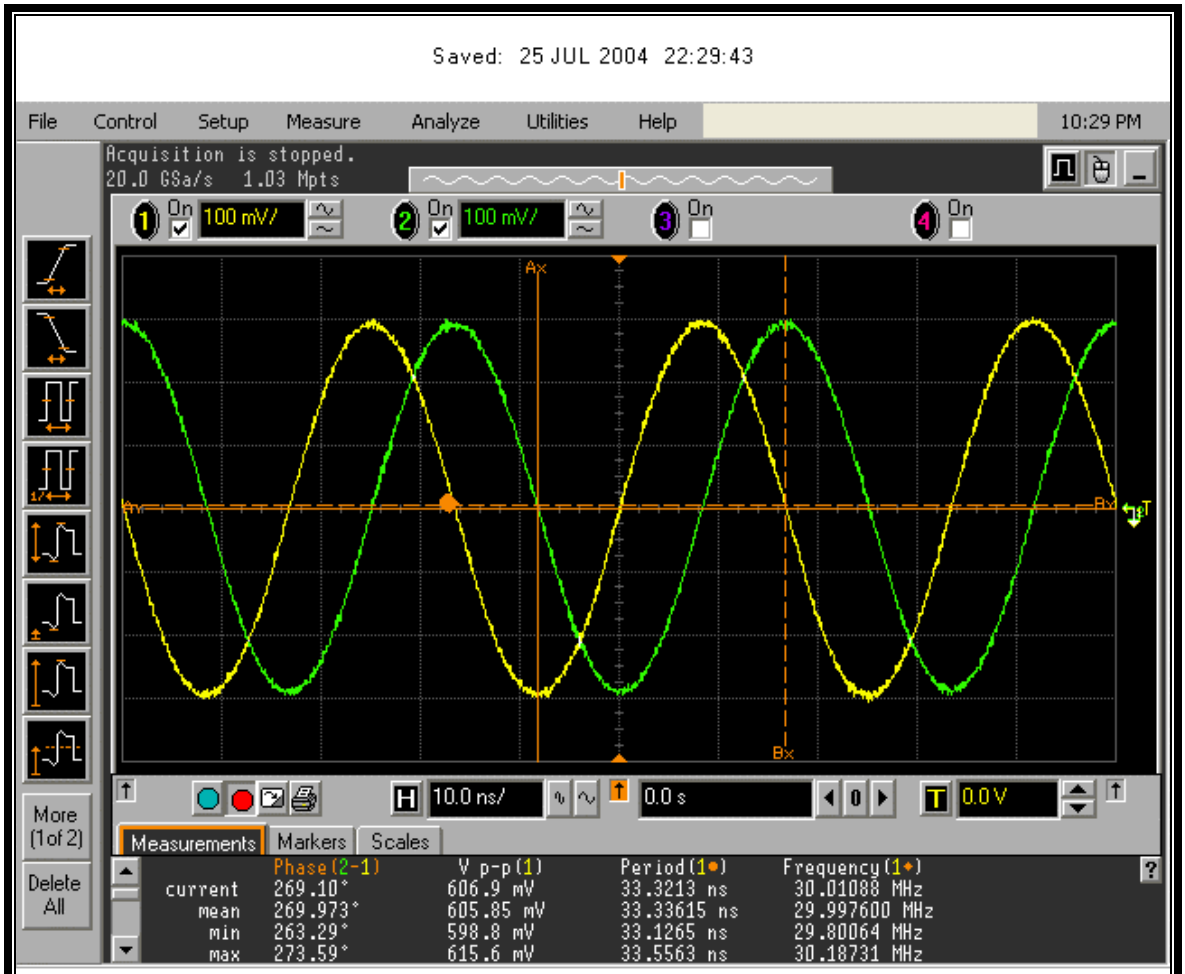
Testing:

Sixteen QD boards were completed and tested. HP8648C and Rohde & Schwartz 5kHz -3GHz signal generators were used for LO signal and IF signal, repectively. The LO was set to -10dBm and it was running at

twice the carrier frequency. HP8563E spectrometer was used to analyze the frequency content in the output signal (either the I or Q output was hooked up to the spectrometer, and the other output was terminated by 50Ω). Fig. 3 shows an output spectrum when the LO at 800MHz, IF=-28.5dBm at 430MHz, (output signal at 30MHz). It was found that for output of 0dBm, minimum IF input has to be greater than -28.5dBm ($V_{control}$=0.2V/maximum gain).

Figure 3: Spectrum output

The phase error of a board was tested using Agilent Infinium 54855A 20Gbits/s oscilloscope. The I/Q outputs were hooked up to the channel 2/channel 1 of the oscilloscope, respectively. The LO was set to -10dBm at 800MHz, and IF was set 430MHz (output at 30MHz). The output signal was adjusted to be 300mV (on 50Ω termination). The phase difference was acquired using the phase function. Fig. 4 shows the snap shot of the oscilloscope screen while the phase difference was acquired. As seen on the screen, the phase mean is 269.10 degrees (=90.90 degrees). Therefore, the error is 0.9 degrees.



Acquisition Sampling mode real time
Memory depth manual 1025000 pts
Sampling rate manual Sampling rate 20.0 GSa/s
Averaging off Interpolation off

Channel 1 Scale 100 mV/ Offset 0.0 V Coupling DC Impedance 50 Ohms

Channel 2 Scale 100 mV/ Offset -3 mV Coupling DC Impedance 50 Ohms

Time base Scale 10.0 ns/ Position 0.0 s Reference center

Trigger Mode edge Sweep auto
Sensitivity low Holdoff time 80 ns
Source channel 1 Trigger level 0.0 V Slope rising

Measure

	Phase(2-1)	V p-p(1)	Period(1)	Frequency(1)
current	269.10°	606.9 mV	33.3213 ns	30.01088 MHz
mean	269.973°	605.85 mV	33.33615 ns	29.997600 MHz
min	263.29°	598.8 mV	33.1265 ns	29.80064 MHz
max	273.59°	615.6 mV	33.5563 ns	30.18731 MHz
std dev	1.384°	2.75 mV	71.83 ps	64.631759 kHz
# of meas	558	558	558	558
edge dir	Falling		Falling	Falling

Marker

	Phase(2-1)	X	Y
current	269.10°	A——(2) = -8.1620 ns	-4.0 mV
mean	269.973°	B---(1) = 16.6593 ns	5.9 mV
min	263.29°	Δ = 24.8213 ns	10.0 mV
max	273.59°	1/ΔX = 40.28792061518 MHz	
std dev	1.384°		

Figure 4: Phase measurement

Sixteen DQ boards were built and tested this way. Table 2 shows the phase difference and phase error for 17 boards. (Note: Originally, board 4b had a phase error over 4 degrees, that why 4b' was built to substitute 4b. Later, a faulty SETI filter was substituted on 4b and the phase error went to 1.994 degrees).

Board Alias	Phase	Phase error
0a	269.973	0.027
0b	270.932	0.932
1a	269.245	0.755
1b	269.814	0.186
2a	89.238	0.762
2b	89.347	0.653
3a	89.605	0.395
3b	90.934	0.934
4a	90.968	0.968
4b	91.994	1.994
4b'	268.775	1.225
5a	90.801	0.801
5b	91.302	1.302
6a	91.055	1.055
6b	89.402	0.598
7a	90.885	0.885
7b	90.645	0.645

Table 2: Phase errors for 17 QD boards.

Summary:

Sixteen QD boards were built and tested for the GALFA project. It was experimentally found that the -3dB point of SETI filters was 38MHz. All 17 QD boards have quadrature phase error under 2.0 degrees. The board has enough gain to amplify an IF signal of -28.5dBm to 0dBm at the output.

If you have any questions about this report, please e-mail me: pmonat@umich.edu