Both JTAG ports are 2.5V

J203
XIL-PLAT-CABLE
2_5V_FPGA:1
GND
Vref/Vref
PROG/TMS
TMS
CCLK/TCK
TCK
Done/TDO
TDO_PORT
Din/TDI
TDI_PORT
NC/NC
INIT/NC

R221 10
TDI_PORT
TDI_CPLD
R222 10
TDO_CPLD
TDI_FPGA
R223 10
TDO_FPGA
TDO_PORT
R224 NONE
TDI_PORT
TDI_FPGA
R225 NONE
TDO_FPGA
TDI_CPLD
R226 NONE
TDO_CPLD
TDO_PORT

TMS
TDO_FPGA
TDI_FPGA
TCK
10K
R206
XC3SXX00FG456-JTAG
U1

2_5V_FPGA:1
DVDD_FPGA:1
R231 130K
R232 NONE
R233 100K
8200pF
C206
C207
0.1uF
U24
RSTin/MRn
SWT
SRT
RESETn
WDI
WDS
MAX6749KA+T
2_5V_FPGA:8
GND:4
POR
WDI
R234 NONE
2_5V_FPGA:1
R203 10K
pg1
R229 NONE
POR
C201 NONE

U11
24Cxx
A0
A1
A2
n/c
SCL
SDA
SCL
SDA
24LC024/SN
DVDD_FPGA:8
GND:4

U10
XC9572-VQ44-IO
2_5V_FPGA:1
0
R211
330
R213
0
R210
POR
cpld_detached
cpld_misc
IO_B1MC2
IO_B1MC5
IO_B1MC6
IO_B1MC8
IO_B1MC9/GCK1
IO_B1MC11/GCK2
IO_B1MC14/GCK3
IO_B1MC15
IO_B1MC17
IO_B2MC2
IO_B2MC5
IO_B2MC6
IO_B2MC8
IO_B2MC9/GSR
IO_B2MC11/GTS2
IO_B2MC14/GTS1
IO_B2MC15
IO_B2MC17
IO_B3MC2
IO_B3MC5
IO_B3MC8
IO_B3MC9
IO_B3MC11
IO_B3MC14
IO_B3MC15
IO_B3MC16
IO_B3MC17
IO_B4MC2
IO_B4MC5
IO_B4MC8
IO_B4MC11
IO_B4MC14
IO_B4MC15
IO_B4MC17
CLK_25MHZ
CLK_25MHZ_EN
cpld_clk
cpld_start
cpld_mode
cpld_done
sd_prot
sd_cs_25
sd_din_25
sd_clk_25
sd_det
ser_loopen
ser_prbsen
cpld_din
2_5V_FPGA:1
4.7K
R212
cpld_init_b
TDI
TDO
TCK
TMS
TDI_CPLD
TDO_CPLD
TCK
TMS

2_5V_FPGA:1
1K
R202
1K
R201
1K
R214
D201
D202
LED1
slot=1

U1
XC3SXX00FG456-CFG
J204
PROG_B
M2
M1
M0
HSWAP_EN
DONE
CCLK
IO_L31P_5/D5
IO_L31P_4/DOUT/BUSY
IO_L31N_5/D4
IO_L31N_4/INIT_B
IO_L30P_4/D3
IO_L30N_4/D2
IO_L28P_5/D7
IO_L28N_5/D6
IO_L27P_4/D1
IO_L27N_4/DIN/D0
IO_L01P_5/CS_B
IO_L01N_5/RDWR_B
V11 cpld_detached
Y12 cpld_misc
W11 ser_enable
W12
V12 cpld_done
U12 cpld_mode
AA9 cpld_start
AB9 ser_rx_en
AB14 cpld_clk
AA14
AA3
Y4 ser_loopen

U10
XC9572-VQ44-PWR
2_5V_FPGA:1
DVDD_FPGA:1
VccO
VccINT
VccINT
GND
GND
GND
C203 0.1uF
C202 0.1uF
C204 0.1uF
C205 0.1uF

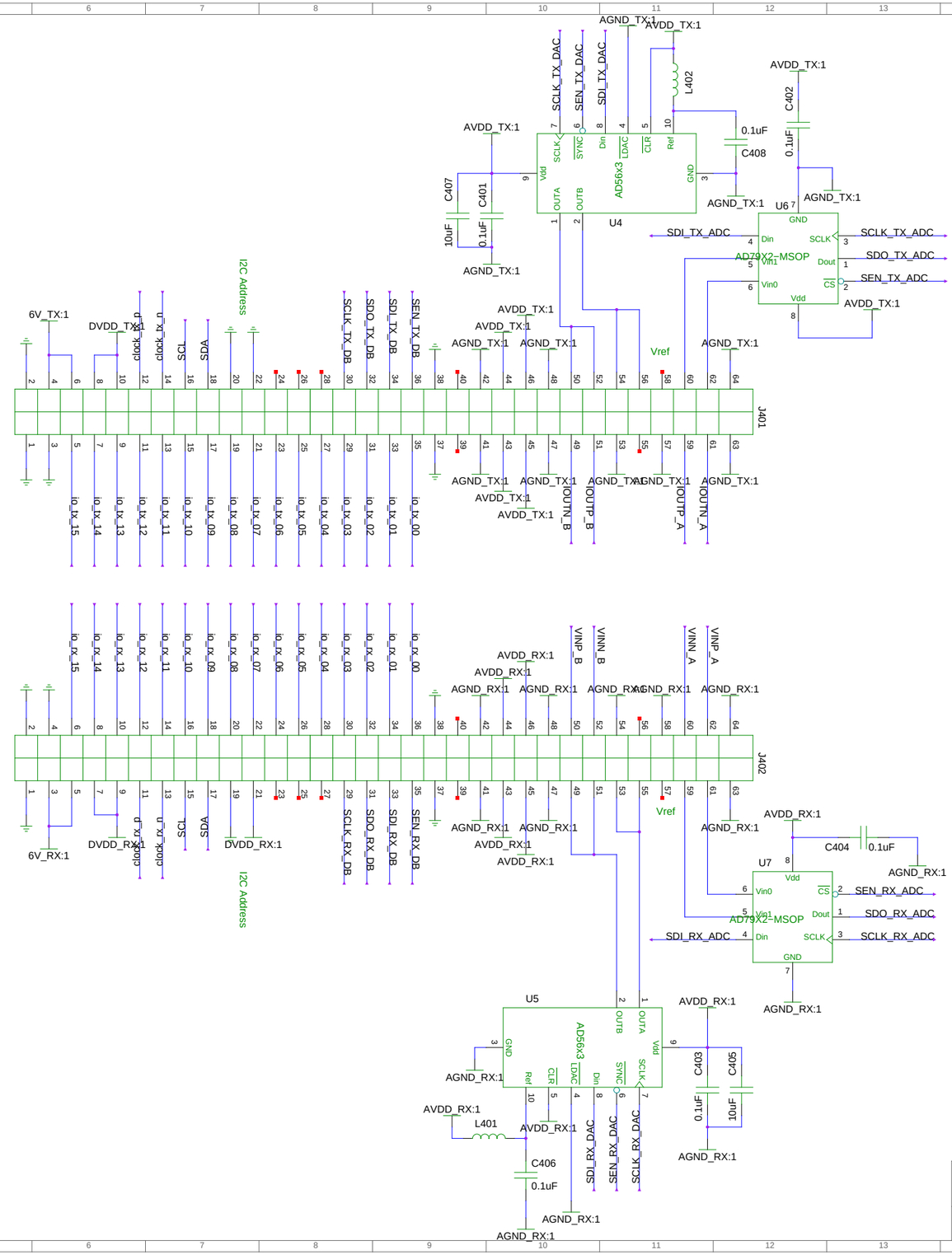
J201
CD_DAT[3]/NC/nCS
CMD/CMD/Din
Vss1
Vdd
CLK
Vss2
DAT[0]/DAT[0]/Dout
DAT[1]/NC/NC
DAT[2]/NC/NC
GND
GND
Pin Defs:
SD/MMC/SPI
sd_cs_33
sd_din_33
sd_clk_33
DVDD_FPGA:1
2_5V_FPGA:1
prot_det_com
protect
detect
sd_prot
sd_det
R228 10K
R227 10K

Slave Serial 2.5V
Bank 4 must be 2.5V

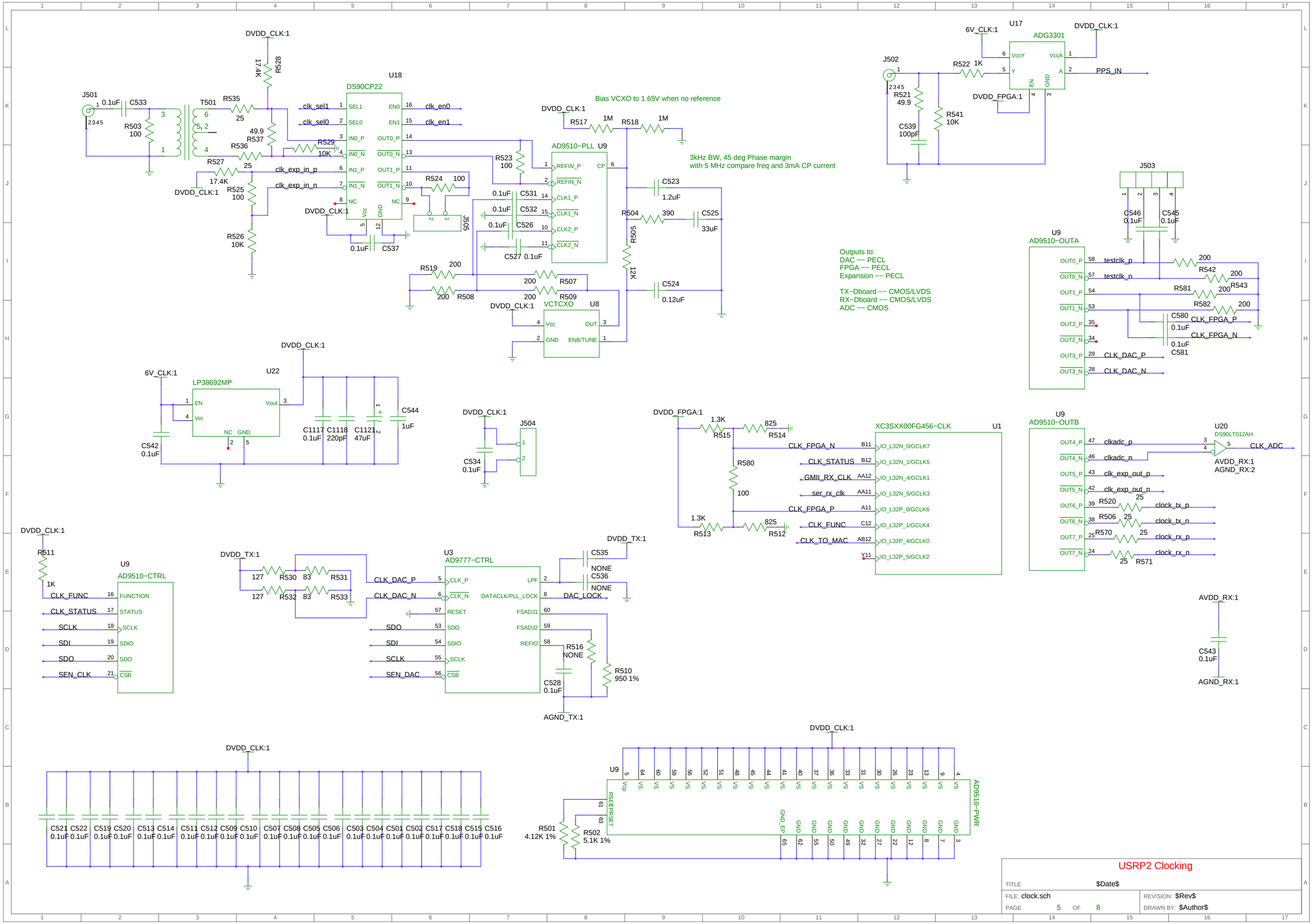
U31
SN74AUP1T57
sd_cs_25
sd_cs_33
U32
SN74AUP1T57
sd_din_25
sd_din_33
U33
SN74AUP1T57
sd_clk_25
sd_clk_33
DVDD_FPGA:1
A
B
C
Y
Vcc
GND

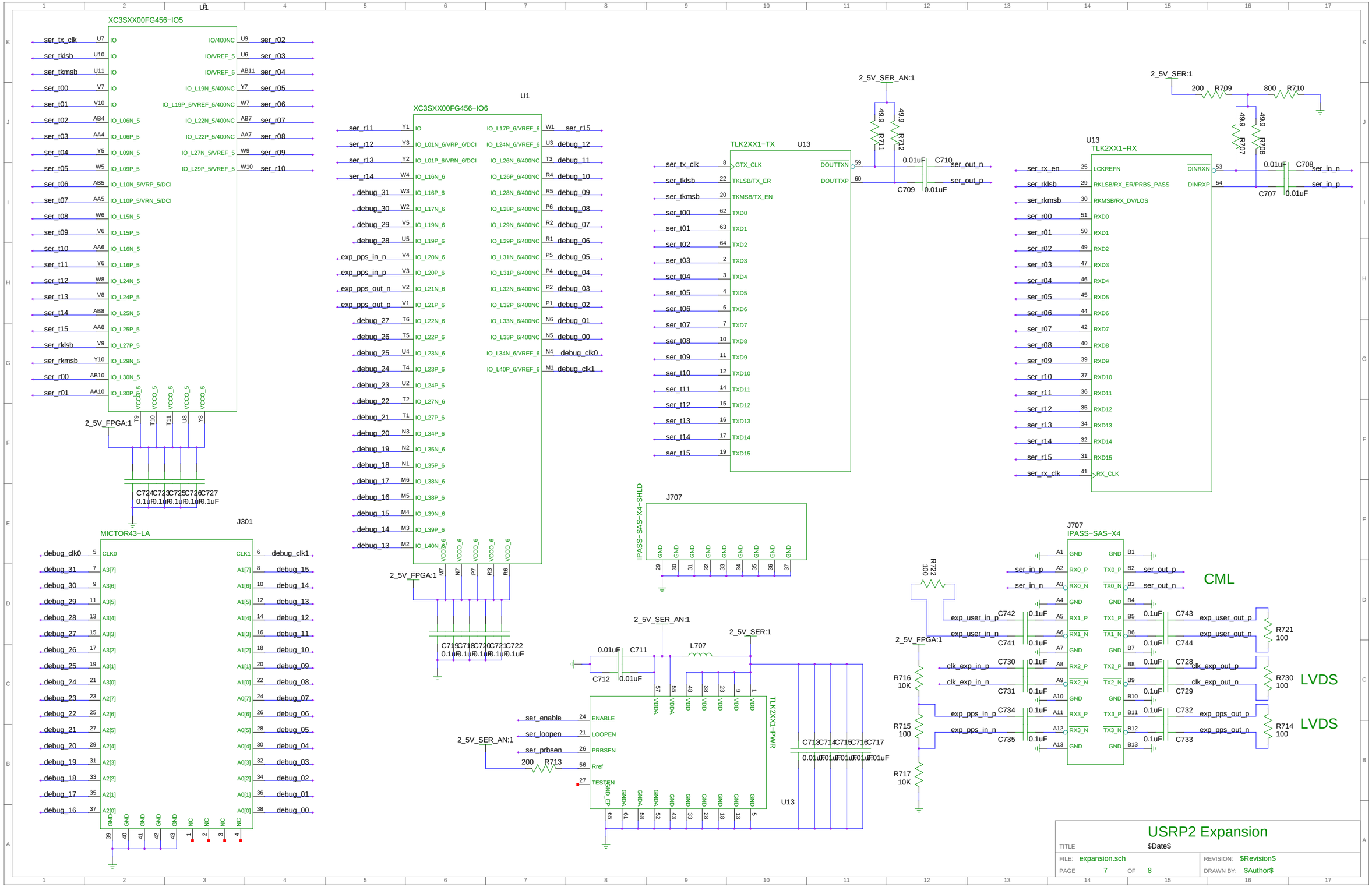
USRP2 Configuration

TITLE	$Date$
FILE: config.sch	REVISION: $Revision$
PAGE 2 OF 8	DRAWN BY: $Author$



USRP2 Daughterboad Interface	
TITLE: $Date$	
FILE: dboard.sch	REVISION: $Revision$
PAGE 4 OF 8	DRAWN BY: $Author$


DVDD_CLK:1
17.4K
R528
U18
DS90CP22
J501
0.1uF
C533
T501
R535
25
clk_sel1
clk_sel0
clk_en0
clk_en1
49.9
R537
R529
10K
R536
R527
25
clk_exp_in_p
clk_exp_in_n
17.4K
R525
100
R526
10K
R503
100
R524
100
J505
0.1uF
C537
Bias VCXO to 1.65V when no reference
R517
1M
R518
1M
AD9510-PLL
U9
R523
100
0.1uF
C531
0.1uF
C532
0.1uF
C526
C527
0.1uF
3kHz BW, 45 deg Phase margin
with 5 MHz compare freq and 3mA CP current
C523
1.2uF
R504
390
C525
33uF
R505
12K
C524
0.12uF
R519
200
R508
200
R507
200
R509
200
VCTCXO
U8
Outputs to:
DAC -- PECL
FPGA -- PECL
Expansion -- PECL
TX-Dboard -- CMOS/LVDS
RX-Dboard -- CMOS/LVDS
ADC -- CMOS
6V_CLK:1
U17
ADG3301
J502
R522
1K
R521
49.9
C539
100pF
R541
10K
PPS_IN
J503
C546
0.1uF
C545
0.1uF
U9
AD9510-OUTA
testclk_p
testclk_n
R542
200
R543
200
R581
200
R582
200
C580
0.1uF
CLK_FPGA_P
CLK_FPGA_N
0.1uF
C581
CLK_DAC_P
CLK_DAC_N
6V_CLK:1
U22
LP38692MP
C542
0.1uF
C1117
0.1uF
C1118
220pF
C1121
47uF
C544
1uF
J504
C534
0.1uF
DVDD_FPGA:1
1.3K
R515
825
R514
R580
100
1.3K
R513
825
R512
XC3SXX00FG456-CLK
U1
CLK_FPGA_N
CLK_STATUS
GMII_RX_CLK
ser_rx_clk
CLK_FPGA_P
CLK_FUNC
CLK_TO_MAC
U9
AD9510-OUTB
clkadc_p
clkadc_n
clk_exp_out_p
clk_exp_out_n
R520
25
R506
25
R570
25
R571
25
clock_tx_p
clock_tx_n
clock_rx_p
clock_rx_n
U20
DS90LT012AH
CLK_ADC
AVDD_RX:1
AGND_RX:2
DVDD_CLK:1
R511
1K
U9
AD9510-CTRL
CLK_FUNC
CLK_STATUS
SCLK
SDI
SDO
SEN_CLK
DVDD_TX:1
127
R530
83
R531
127
R532
83
R533
U3
AD9777-CTRL
CLK_DAC_P
CLK_DAC_N
SDO
SDI
SCLK
SEN_DAC
C535
NONE
C536
NONE
DATACLK/PLL_LOCK
DAC_LOCK
R516
NONE
C528
0.1uF
R510
950 1%
AGND_TX:1
AVDD_RX:1
C543
0.1uF
AGND_RX:1
C521 C522 C519 C520 C513 C514 C511 C512 C509 C510 C507 C508 C505 C506 C503 C504 C501 C502 C517 C518 C515 C516
0.1uF
U9
AD9510-PWR
R501
4.12K 1%
R502
5.1K 1%
USRP2 Clocking
TITLE $Date$
FILE: clock.sch
REVISION: Rev
PAGE 5 OF 8
DRAWN BY: $Author$


U1
XC3SXX00FG456-IO5
ser_tx_clk U7 IO
ser_tklsb U10 IO
ser_tkmsb U11 IO
ser_t00 V7 IO
ser_t01 V10 IO
ser_t02 AB4 IO_L06N_5
ser_t03 AA4 IO_L06P_5
ser_t04 Y5 IO_L09N_5
ser_t05 W5 IO_L09P_5
ser_t06 AB5 IO_L10N_5/VRP_5/DCI
ser_t07 AA5 IO_L10P_5/VRN_5/DCI
ser_t08 W6 IO_L15N_5
ser_t09 V6 IO_L15P_5
ser_t10 AA6 IO_L16N_5
ser_t11 Y6 IO_L16P_5
ser_t12 W8 IO_L24N_5
ser_t13 V8 IO_L24P_5
ser_t14 AB8 IO_L25N_5
ser_t15 AA8 IO_L25P_5
ser_rklsb V9 IO_L27P_5
ser_rkmsb Y10 IO_L29N_5
ser_r00 AB10 IO_L30N_5
ser_r01 AA10 IO_L30P_5
IO/400NC U9 ser_r02
IO/VREF_5 U6 ser_r03
IO/VREF_5 AB11 ser_r04
IO_L19N_5/400NC Y7 ser_r05
IO_L19P_5/VREF_5/400NC W7 ser_r06
IO_L22N_5/400NC AB7 ser_r07
IO_L22P_5/400NC AA7 ser_r08
IO_L27N_5/VREF_5 W9 ser_r09
IO_L29P_5/VREF_5 W10 ser_r10
VCCO_5 T9 T10 T11 U8 Y8
2_5V_FPGA:1
C724 0.1uF C723 0.1uF C725 0.1uF C726 0.1uF C727 0.1uF
J301
MICTOR43-LA
debug_clk0 5 CLK0
debug_31 7 A3[7]
debug_30 9 A3[6]
debug_29 11 A3[5]
debug_28 13 A3[4]
debug_27 15 A3[3]
debug_26 17 A3[2]
debug_25 19 A3[1]
debug_24 21 A3[0]
debug_23 23 A2[7]
debug_22 25 A2[6]
debug_21 27 A2[5]
debug_20 29 A2[4]
debug_19 31 A2[3]
debug_18 33 A2[2]
debug_17 35 A2[1]
debug_16 37 A2[0]
CLK1 6 debug_clk1
A1[7] 8 debug_15
A1[6] 10 debug_14
A1[5] 12 debug_13
A1[4] 14 debug_12
A1[3] 16 debug_11
A1[2] 18 debug_10
A1[1] 20 debug_09
A1[0] 22 debug_08
A0[7] 24 debug_07
A0[6] 26 debug_06
A0[5] 28 debug_05
A0[4] 30 debug_04
A0[3] 32 debug_03
A0[2] 34 debug_02
A0[1] 36 debug_01
A0[0] 38 debug_00
GND 39 GND 40 GND 41 GND 42 GND 43 NC 1 NC 2 NC 3 NC 4
U1
XC3SXX00FG456-IO6
ser_r11 Y1 IO
ser_r12 Y3 IO_L01N_6/VRP_6/DCI
ser_r13 Y2 IO_L01P_6/VRN_6/DCI
ser_r14 W4 IO_L16N_6
debug_31 W3 IO_L16P_6
debug_30 W2 IO_L17N_6
debug_29 V5 IO_L19N_6
debug_28 U5 IO_L19P_6
exp_pps_in_n V4 IO_L20N_6
exp_pps_in_p V3 IO_L20P_6
exp_pps_out_n V2 IO_L21N_6
exp_pps_out_p V1 IO_L21P_6
debug_27 T6 IO_L22N_6
debug_26 T5 IO_L22P_6
debug_25 U4 IO_L23N_6
debug_24 T4 IO_L23P_6
debug_23 U2 IO_L24P_6
debug_22 T2 IO_L27N_6
debug_21 T1 IO_L27P_6
debug_20 N3 IO_L34P_6
debug_19 N2 IO_L35N_6
debug_18 N1 IO_L35P_6
debug_17 M6 IO_L38N_6
debug_16 M5 IO_L38P_6
debug_15 M4 IO_L39N_6
debug_14 M3 IO_L39P_6
debug_13 M2 IO_L40N_6
IO_L17P_6/VREF_6 W1 ser_r15
IO_L24N_6/VREF_6 U3 debug_12
IO_L26N_6/400NC T3 debug_11
IO_L26P_6/400NC R4 debug_10
IO_L28N_6/400NC R5 debug_09
IO_L28P_6/400NC P6 debug_08
IO_L29N_6/400NC R2 debug_07
IO_L29P_6/400NC R1 debug_06
IO_L31N_6/400NC P5 debug_05
IO_L31P_6/400NC P4 debug_04
IO_L32N_6/400NC P2 debug_03
IO_L32P_6/400NC P1 debug_02
IO_L33N_6/400NC N6 debug_01
IO_L33P_6/400NC N5 debug_00
IO_L34N_6/VREF_6 N4 debug_clk0
IO_L40P_6/VREF_6 M1 debug_clk1
VCCO_6 M7 N7 P7 R3 R6
2_5V_FPGA:1
C719 0.1uF C718 0.1uF C720 0.1uF C721 0.1uF C722 0.1uF
2_5V_SER_AN:1
TLK2XX1-TX
U13
ser_tx_clk 8 GTX_CLK
ser_tklsb 22 TKLSB/TX_ER
ser_tkmsb 20 TKMSB/TX_EN
ser_t00 62 TXD0
ser_t01 63 TXD1
ser_t02 64 TXD2
ser_t03 2 TXD3
ser_t04 3 TXD4
ser_t05 4 TXD5
ser_t06 6 TXD6
ser_t07 7 TXD7
ser_t08 10 TXD8
ser_t09 11 TXD9
ser_t10 12 TXD10
ser_t11 14 TXD11
ser_t12 15 TXD12
ser_t13 16 TXD13
ser_t14 17 TXD14
ser_t15 19 TXD15
DOUTTXN 59
DOUTTXP 60
49.9 R711
49.9 R712
0.01uF C710 ser_out_n
0.01uF C709 ser_out_p
J707
IPASS-SAS-X4-SHLD
GND 29 GND 30 GND 31 GND 32 GND 33 GND 34 GND 35 GND 36 GND 37
2_5V_SER_AN:1
2_5V_SER:1
0.01uF C712
C711 0.01uF
L707
ser_enable 24 ENABLE
ser_loopen 21 LOOPEN
ser_prbsen 26 PRBSEN
Rref 56
TESTEN 27
VDDA 57 VDDA 55
VDD 48 VDD 38 VDD 23 VDD 9 VDD 1
GND_EP 65 GNDA 61 GNDA 58 GNDA 52 GND 43 GND 33 GND 28 GND 18 GND 13 GND 5
TLK2X1-PWR
2_5V_SER_AN:1
200 R713
C713 0.01uF C714 0.01uF C715 0.01uF C716 0.01uF C717 0.01uF
U13
2_5V_SER:1
200 R709 800 R710
49.9 R707
49.9 R708
0.01uF C708 ser_in_n
0.01uF C707 ser_in_p
U13
TLK2XX1-RX
ser_rx_en 25 LCKREFN
ser_rklsb 29 RKLSB/RX_ER/PRBS_PASS
ser_rkmsb 30 RKMSB/RX_DV/LOS
ser_r00 51 RXD0
ser_r01 50 RXD1
ser_r02 49 RXD2
ser_r03 47 RXD3
ser_r04 46 RXD4
ser_r05 45 RXD5
ser_r06 44 RXD6
ser_r07 42 RXD7
ser_r08 40 RXD8
ser_r09 39 RXD9
ser_r10 37 RXD10
ser_r11 36 RXD11
ser_r12 35 RXD12
ser_r13 34 RXD13
ser_r14 32 RXD14
ser_r15 31 RXD15
ser_rx_clk 41 RX_CLK
DINRXN 53
DINRXP 54
J707
IPASS-SAS-X4
R722 100
2_5V_FPGA:1
R716 10K
R715 100
R717 10K
CML
exp_user_in_p C742 0.1uF
exp_user_in_n C741 0.1uF
clk_exp_in_p C730 0.1uF
clk_exp_in_n C731 0.1uF
exp_pps_in_p C734 0.1uF
exp_pps_in_n C735 0.1uF
A1 GND A2 RX0_P A3 RX0_N A4 GND A5 RX1_P A6 RX1_N A7 GND A8 RX2_P A9 RX2_N A10 GND A11 RX3_P A12 RX3_N A13 GND
GND B1 TX0_P B2 ser_out_p TX0_N B3 ser_out_n GND B4 TX1_P B5 0.1uF C743 exp_user_out_p TX1_N B6 exp_user_out_n GND B7 TX2_P B8 0.1uF C728 clk_exp_out_p TX2_N B9 clk_exp_out_n GND B10 TX3_P B11 0.1uF C732 exp_pps_out_p TX3_N B12 exp_pps_out_n GND B13
0.1uF C744
0.1uF C729
0.1uF C733
R721 100
R730 100
R714 100
LVDS
LVDS
USRP2 Expansion
TITLE $Date$
FILE: expansion.sch
REVISION: $Revision$
PAGE 7 OF 8
DRAWN BY: $Author$

Add caps at 2.5V near PHY

LED Polarities!!!
Section 5.9

Everything on 2.5V

U1
XC3SXX00FG456-IO4

U12
DP83865-MDI

J601
BEL 0826-1X1T-23-F

U12
DP83865-JTAG

U12
DP83865-PWR

U12
DP83865-MAC

U12
DP83865-MGT

U12
DP83865-CLK

U12
DP83865-CFGLED

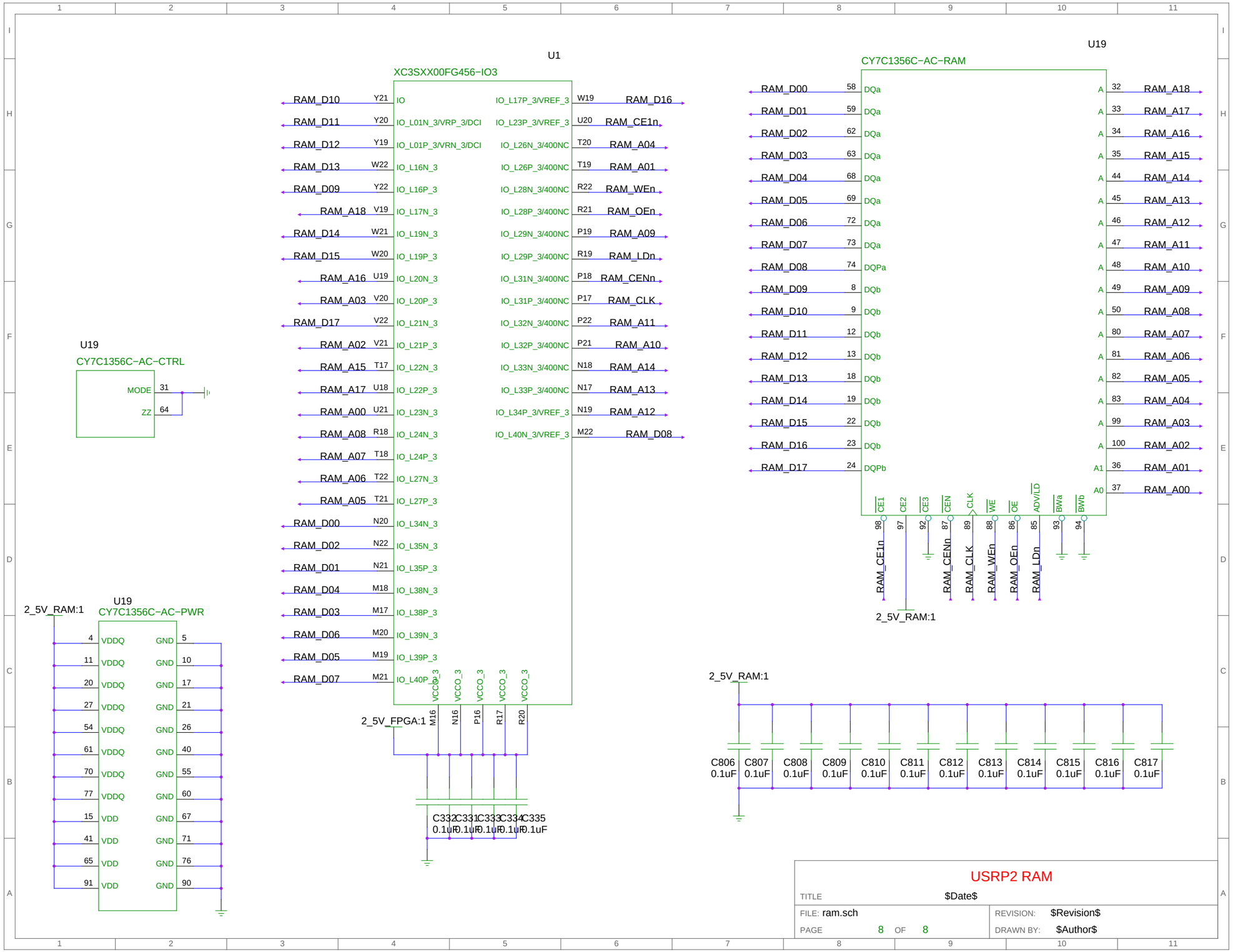
VCTCXO X2

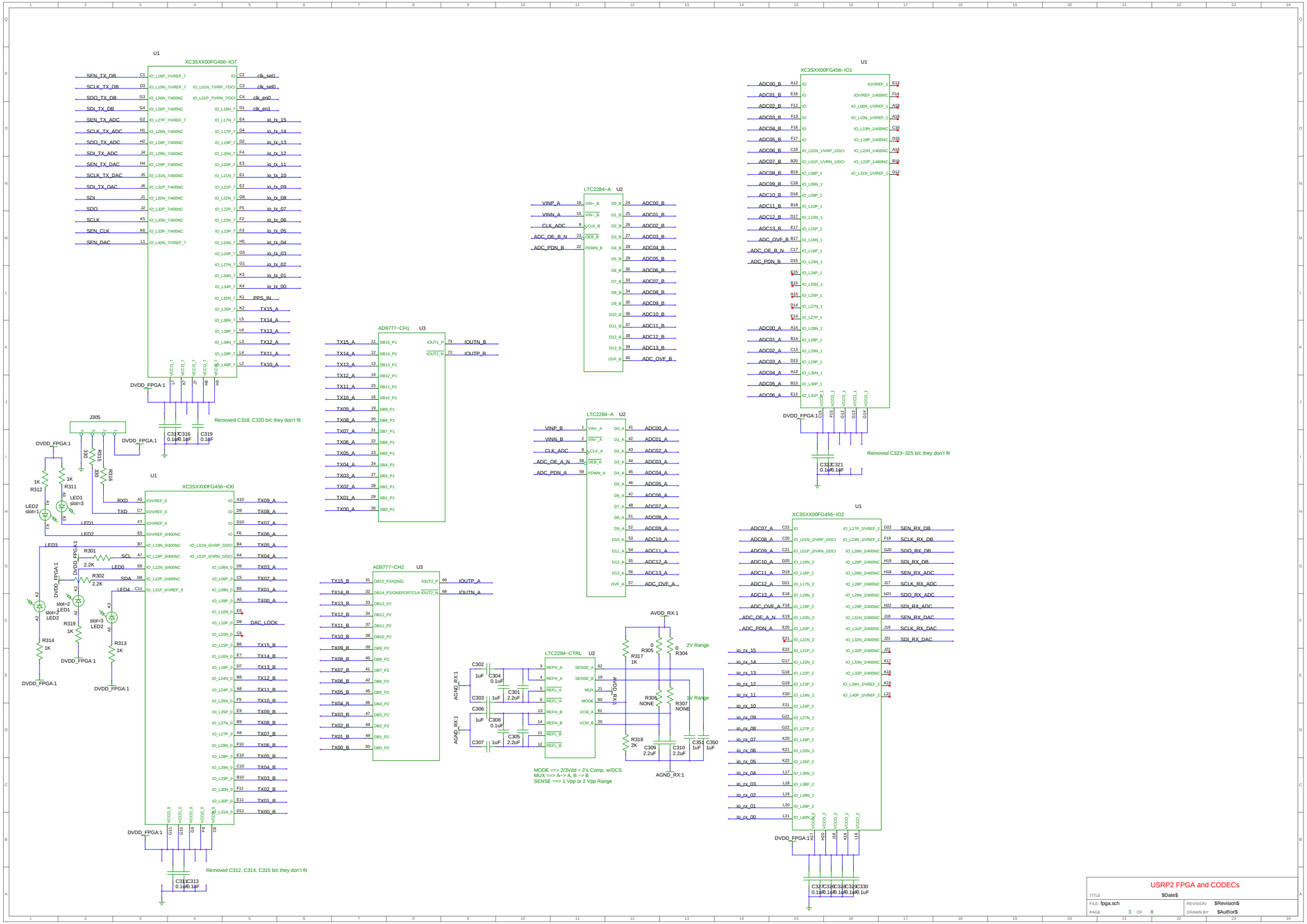
2_5V_ETH:1
2_5V_FPGA:1
2_5V_ETH_A:1
1_8V:1
1_8VA:1

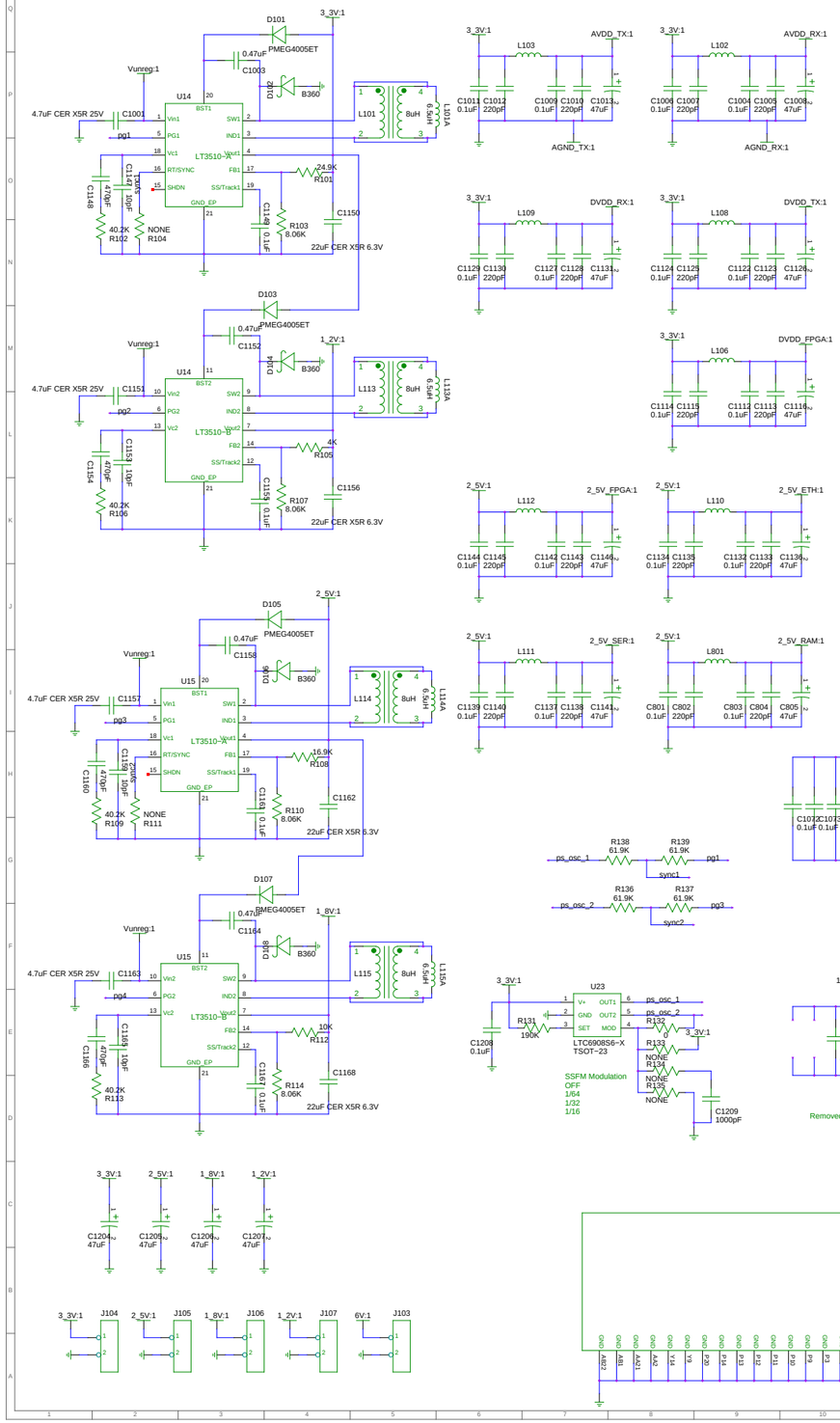
CHASSIS_GND:1

USRP2 Ethernet

TITLE	$Date$
FILE: ethernet.sch	REVISION: $Revision$
PAGE 6 OF 8	DRAWN BY: $Author$


U1
XC3SXX00FG456-IO3
RAM_D10 Y21 IO
RAM_D11 Y20 IO_L01N_3/VRP_3/DCI
RAM_D12 Y19 IO_L01P_3/VRN_3/DCI
RAM_D13 W22 IO_L16N_3
RAM_D09 Y22 IO_L16P_3
RAM_A18 V19 IO_L17N_3
RAM_D14 W21 IO_L19N_3
RAM_D15 W20 IO_L19P_3
RAM_A16 U19 IO_L20N_3
RAM_A03 V20 IO_L20P_3
RAM_D17 V22 IO_L21N_3
RAM_A02 V21 IO_L21P_3
RAM_A15 T17 IO_L22N_3
RAM_A17 U18 IO_L22P_3
RAM_A00 U21 IO_L23N_3
RAM_A08 R18 IO_L24N_3
RAM_A07 T18 IO_L24P_3
RAM_A06 T22 IO_L27N_3
RAM_A05 T21 IO_L27P_3
RAM_D00 N20 IO_L34N_3
RAM_D02 N22 IO_L35N_3
RAM_D01 N21 IO_L35P_3
RAM_D04 M18 IO_L38N_3
RAM_D03 M17 IO_L38P_3
RAM_D06 M20 IO_L39N_3
RAM_D05 M19 IO_L39P_3
RAM_D07 M21 IO_L40P_3
IO_L17P_3/VREF_3 W19 RAM_D16
IO_L23P_3/VREF_3 U20 RAM_CE1n
IO_L26N_3/400NC T20 RAM_A04
IO_L26P_3/400NC T19 RAM_A01
IO_L28N_3/400NC R22 RAM_WEn
IO_L28P_3/400NC R21 RAM_OEn
IO_L29N_3/400NC P19 RAM_A09
IO_L29P_3/400NC R19 RAM_LDn
IO_L31N_3/400NC P18 RAM_CENn
IO_L31P_3/400NC P17 RAM_CLK
IO_L32N_3/400NC P22 RAM_A11
IO_L32P_3/400NC P21 RAM_A10
IO_L33N_3/400NC N18 RAM_A14
IO_L33P_3/400NC N17 RAM_A13
IO_L34P_3/VREF_3 N19 RAM_A12
IO_L40N_3/VREF_3 M22 RAM_D08
VCCO_3 M16
VCCO_3 N16
VCCO_3 P16
VCCO_3 R17
VCCO_3 R20
2_5V_FPGA:1
C332 0.1uF
C331 0.1uF
C333 0.1uF
C334 0.1uF
C335 0.1uF
U19
CY7C1356C-AC-CTRL
MODE 31
ZZ 64
U19
2_5V_RAM:1
CY7C1356C-AC-PWR
4 VDDQ
11 VDDQ
20 VDDQ
27 VDDQ
54 VDDQ
61 VDDQ
70 VDDQ
77 VDDQ
15 VDD
41 VDD
65 VDD
91 VDD
GND 5
GND 10
GND 17
GND 21
GND 26
GND 40
GND 55
GND 60
GND 67
GND 71
GND 76
GND 90
U19
CY7C1356C-AC-RAM
RAM_D00 58 DQa
RAM_D01 59 DQa
RAM_D02 62 DQa
RAM_D03 63 DQa
RAM_D04 68 DQa
RAM_D05 69 DQa
RAM_D06 72 DQa
RAM_D07 73 DQa
RAM_D08 74 DQPa
RAM_D09 8 DQb
RAM_D10 9 DQb
RAM_D11 12 DQb
RAM_D12 13 DQb
RAM_D13 18 DQb
RAM_D14 19 DQb
RAM_D15 22 DQb
RAM_D16 23 DQb
RAM_D17 24 DQPb
A 32 RAM_A18
A 33 RAM_A17
A 34 RAM_A16
A 35 RAM_A15
A 44 RAM_A14
A 45 RAM_A13
A 46 RAM_A12
A 47 RAM_A11
A 48 RAM_A10
A 49 RAM_A09
A 50 RAM_A08
A 80 RAM_A07
A 81 RAM_A06
A 82 RAM_A05
A 83 RAM_A04
A 99 RAM_A03
A 100 RAM_A02
A1 36 RAM_A01
A0 37 RAM_A00
CE1 98 RAM_CE1n
CE2 97
CE3 92
CEN 87 RAM_CENn
CLK 89 RAM_CLK
WE 88 RAM_WEn
OE 86 RAM_OEn
ADV/LD 85 RAM_LDn
BWa 93
BWb 94
2_5V_RAM:1
2_5V_RAM:1
C806 0.1uF
C807 0.1uF
C808 0.1uF
C809 0.1uF
C810 0.1uF
C811 0.1uF
C812 0.1uF
C813 0.1uF
C814 0.1uF
C815 0.1uF
C816 0.1uF
C817 0.1uF
USRP2 RAM
TITLE $Date$
FILE: ram.sch
REVISION: $Revision$
PAGE 8 OF 8
DRAWN BY: $Author$


U1
XC3SXX00FG456-IO7
SEN_TX_DB
SCLK_TX_DB
SDO_TX_DB
SDI_TX_DB
SEN_TX_ADC
SCLK_TX_ADC
SDO_TX_ADC
SDI_TX_ADC
SEN_TX_DAC
SCLK_TX_DAC
SDI_TX_DAC
SDI
SDO
SCLK
SEN_CLK
SEN_DAC
clk_sel1
clk_sel0
clk_en0
clk_en1
io_tx_15
io_tx_14
io_tx_13
io_tx_12
io_tx_11
io_tx_10
io_tx_09
io_tx_08
io_tx_07
io_tx_06
io_tx_05
io_tx_04
io_tx_03
io_tx_02
io_tx_01
io_tx_00
PPS_IN
TX15_A
TX14_A
TX13_A
TX12_A
TX11_A
TX10_A
DVDD_FPGA:1
Removed C318, C320 b/c they don't fit
C317 0.1uF
C316 0.1uF
C319 0.1uF
J305
R315 330
R316 330
R312 1K
R311 1K
LED1 slot=3
LED2 slot=1
LED3
LED0
LED4
R301 2.2K
R302 2.2K
SCL
SDA
R319 1K
R314 1K
R313 1K
DVDD_FPGA:1
U1
XC3SXX00FG456-IO0
RXD
TXD
LED1
LED2
LED3
LED0
LED4
SCL
SDA
DAC_LOCK
TX09_A
TX08_A
TX07_A
TX06_A
TX05_A
TX04_A
TX03_A
TX02_A
TX01_A
TX00_A
TX15_B
TX14_B
TX13_B
TX12_B
TX11_B
TX10_B
TX09_B
TX08_B
TX07_B
TX06_B
TX05_B
TX04_B
TX03_B
TX02_B
TX01_B
TX00_B
DVDD_FPGA:1
Removed C312, C314, C315 b/c they don't fit
C311 0.1uF
C313 0.1uF
AD9777-CH1 U3
IOUTN_B
IOUTP_B
AD9777-CH2 U3
IOUTP_A
IOUTN_A
LTC2284-A U2
ADC00_B
ADC01_B
ADC02_B
ADC03_B
ADC04_B
ADC05_B
ADC06_B
ADC07_B
ADC08_B
ADC09_B
ADC10_B
ADC11_B
ADC12_B
ADC13_B
ADC_OVF_B
LTC2284-A U2
ADC00_A
ADC01_A
ADC02_A
ADC03_A
ADC04_A
ADC05_A
ADC06_A
ADC07_A
ADC08_A
ADC09_A
ADC10_A
ADC11_A
ADC12_A
ADC13_A
ADC_OVF_A
LTC2284-CTRL U2
MODE ==> 2/3Vdd = 2's Comp, w/DCS
MUX ==> A->A, B->B
SENSE ==> 1 Vpp or 2 Vpp Range
AVDD_RX:1
AGND_RX:1
2V Range
1V Range
U1
XC3SXX00FG456-IO1
ADC00_A
ADC01_A
ADC02_A
ADC03_A
ADC04_A
ADC05_A
ADC06_A
ADC07_A
ADC08_A
ADC09_A
ADC10_A
ADC11_A
ADC12_A
ADC13_A
ADC_OVF_A
ADC_OE_A_N
ADC_PDN_A
DVDD_FPGA:1
Removed C323-325 b/c they don't fit
C322 0.1uF
C321 0.1uF
U1
XC3SXX00FG456-IO2
SEN_RX_DB
SCLK_RX_DB
SDO_RX_DB
SDI_RX_DB
SEN_RX_ADC
SCLK_RX_ADC
SDO_RX_ADC
SDI_RX_ADC
SEN_RX_DAC
SCLK_RX_DAC
SDI_RX_DAC
io_rx_15
io_rx_14
io_rx_13
io_rx_12
io_rx_11
io_rx_10
io_rx_09
io_rx_08
io_rx_07
io_rx_06
io_rx_05
io_rx_04
io_rx_03
io_rx_02
io_rx_01
io_rx_00
DVDD_FPGA:1
C327 0.1uF
C326 0.1uF
C328 0.1uF
C329 0.1uF
C330 0.1uF
USRP2 FPGA and CODECs
TITLE $Date$
FILE fpga.sch
REVISION: $Revision$
PAGE 3 OF 8
DRAWN BY: $Author$


D101
3_3V:1
PMEG4005ET
0.47uF
C1003
Vunreg:1
U14
B360
D102
4.7uF CER X5R 25V
C1001
L101
8uH
6.3uH
L101A
pg1
LT3510-A
24.9K
R101
C1149
470pF
C1005
100pF
40.2K
R102
NONE
R104
C1148
0.1uF
R103
8.06K
C1150
22uF CER X5R 6.3V
D103
C1152
1_2V:1
D104
C1151
pg2
LT3510-B
4K
R105
C1153
C1154
R106
C1155
R107
C1156
D105
2_5V:1
C1158
U15
C1157
pg3
C1159
C1160
R109
R111
R108
16.9K
R110
C1162
D107
1_8V:1
C1164
C1163
pg4
C1165
C1166
R113
R112
10K
R114
C1168
3_3V:1
2_5V:1
1_8V:1
1_2V:1
6V:1
J104
J105
J106
J107
J103
L103
AVDD_TX:1
C1011
C1012
220pF
C1009
C1010
C1013
47uF
AGND_TX:1
L102
AVDD_RX:1
C1004
C1005
C1006
AGND_RX:1
L109
DVDD_RX:1
C1129
C1130
C1127
C1128
C1131
L108
DVDD_TX:1
C1124
C1125
C1122
C1123
C1126
L106
DVDD_FPGA:1
C1114
C1115
C1112
C1113
C1116
L112
2_5V_FPGA:1
C1144
C1145
C1142
C1143
C1146
L110
2_5V_ETH:1
C1134
C1135
C1132
C1133
C1136
L111
2_5V_SER:1
C1139
C1140
C1137
C1138
C1141
L801
2_5V_RAM:1
C801
C802
C803
C804
C805
R138
61.9K
R139
ps_osc_1
pg1
sync1
R136
R137
ps_osc_2
pg3
sync2
U23
LTC6908S6-X
TSOT-23
SSFM Modulation
OFF
1/64
1/32
1/16
R131
190K
C1208
0.1uF
R132
R133
R134
R135
NONE
C1209
1000pF
U1
XC3SX00FG484-PWR
1_2V:1
2_5V_FPGA:1
Removed C1025, C1052, C1056, C1057 b/c they don't fit
Removed C1014~C1021 b/c they don't fit
Vunreg:1
L122
C1217
C1203
47uF
C1169
6V:1
6V_CLK:1
L107
C1119
0.1uF
C541
1uF
C540
47uF
6V_TX:1
L119
C1181
C1182
C1183
6V_RX:1
L120
C1184
C1185
C1186
Front Panel Power
J101
C1170
0.47uF
F101
SMD-XXX
L118
L121
F102
C1002
470uF 20V
C1176
J102
ALT Power
FAN Power
F103
500mA
12
R130
4.7uF CER X5R 25V
C1174
0.1uF
C1175
J108
M1
M2
M3
M4
M5
M6
M7
M8
M9
M10
Power Supplies
6V Daughterboard Power (<1A)
3.3VAN LTC2284 (200mA), AD9777 (<500mA)
3.3VCLK AD9510 (<500mA), CLOCK (88mA)
3.3VDIG All IO (<2A)
2.5V FPGA AUX (<100mA), Ethernet Core (<300mA), SERDES (<150mA)
1.8V Ethernet Core (~500mA)
1.2V FPGA Core (<2A)
DVDD_RX:1
AVDD_RX:1
U2
LTC2284-PWR
C1064
C1065
C1058
C1059
C1061
C1060
AGND_RX:1
DVDD_TX:1
AVDD_TX:1
U3
AD9777-PWR
C1072
C1073
C1070
C1071
C1068
C1069
C1066
C1067
C1092
C1093
C1090
C1091
C1088
C1089
AGND_TX:1
USRP2 Power
TITLE: $Date$
FILE: power.sch
REVISION: $Revision$
PAGE: 1 OF 8
DRAWN BY: $Author$